2PASCL: Simulation on logic gates using 1.2μm standard CMOS process

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Abstract

The paper demonstrate the simulation results of 2PASCL NOT, 2NAND, 2NOR, 2XOR and 2AND logic gates using 1.2 μm process. Their power dissipations at 1 to 100 MHz transition frequencies are compared to that of static CMOS topology. Furthermore, simulation results of 2PASCL D-flipflop, half-adder and full-adder are presented. W/L of all the transistors used in the simulations are $5.0\mu/1.2\ \mu$. Load capacitance of 0.1 pF are used.

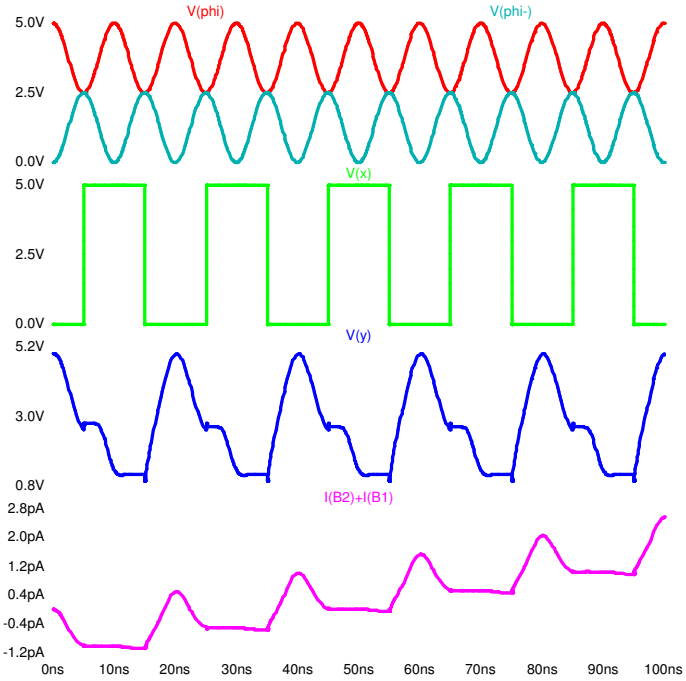

Fig. 1 Output waveforms of 2PASCL NOT using 1.2μ process at 50 MHz f_T.

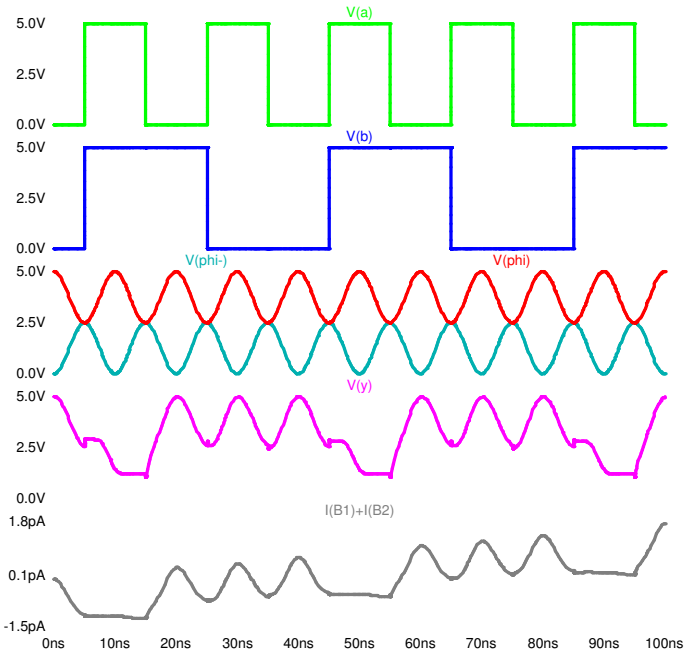

Fig. 2 Output waveforms of 2PASCL 2NAND using 1.2μ process at 50 MHz f_T.

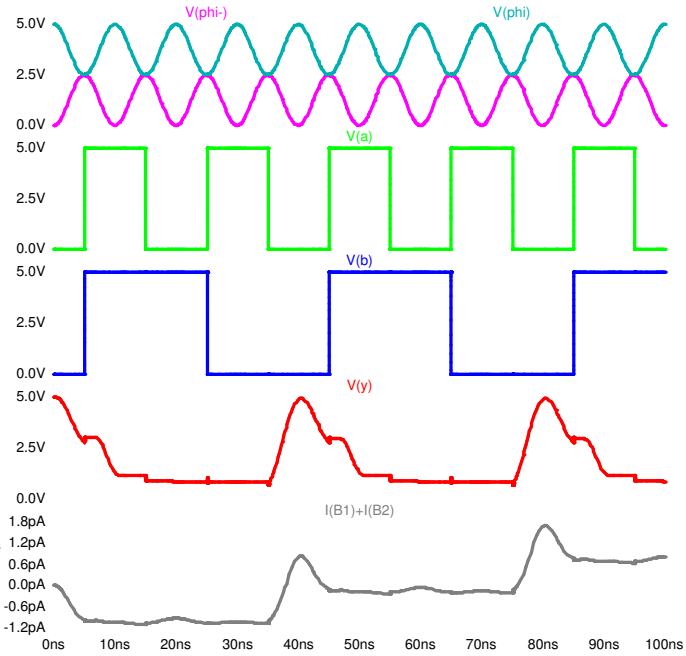

Fig. 3 Output waveforms of 2PASCL 2NOR using 1.2μ process at 50 MHz f_T.

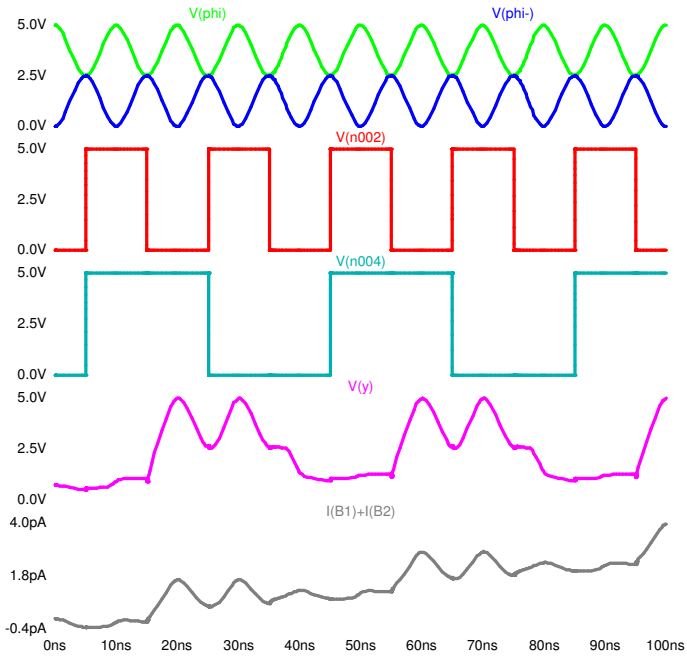

Fig. 4 Output waveforms of 2PASCL 2XOR using 1.2μ process at 50 MHz f_T.

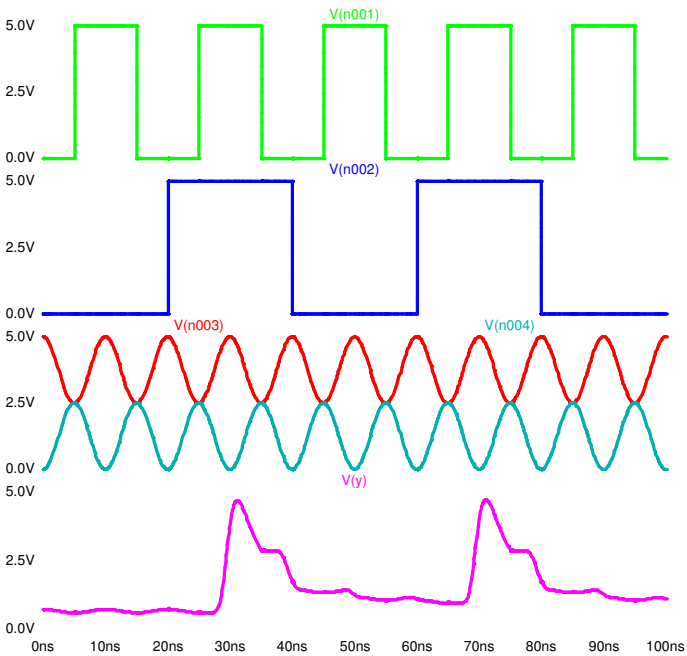

Fig. 5 Output waveforms of 2PASCL 2AND using 1.2μ process at 50 MHz f_T.

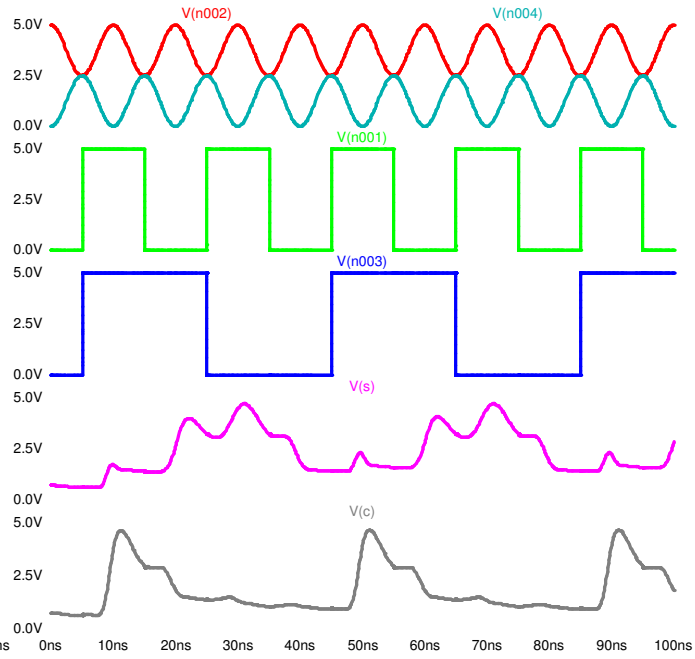

Fig. 6 Output waveforms of 2PASCL half adder using 1.2μ process at 50 MHz f_T.

Fig. 7 Output waveforms of 2PASCL full adder using 1.2μ process at 50 MHz f_T.

2 Results

Table 1 Power dissipation difference results.

Logic	Max. Difference
NOT	-84.8%
NOR	-83.7%
NAND	-87.1%
XOR	-77.4%

3 Conclusion

The SPICE simulation of 2PASCL logics using 1.2μ CMOS procees which leads to the fabrication has been carried. Significant lower power dissipations are seen in all logics. Next, 4x4 bit 2PASCL multiplier simulation will be done.

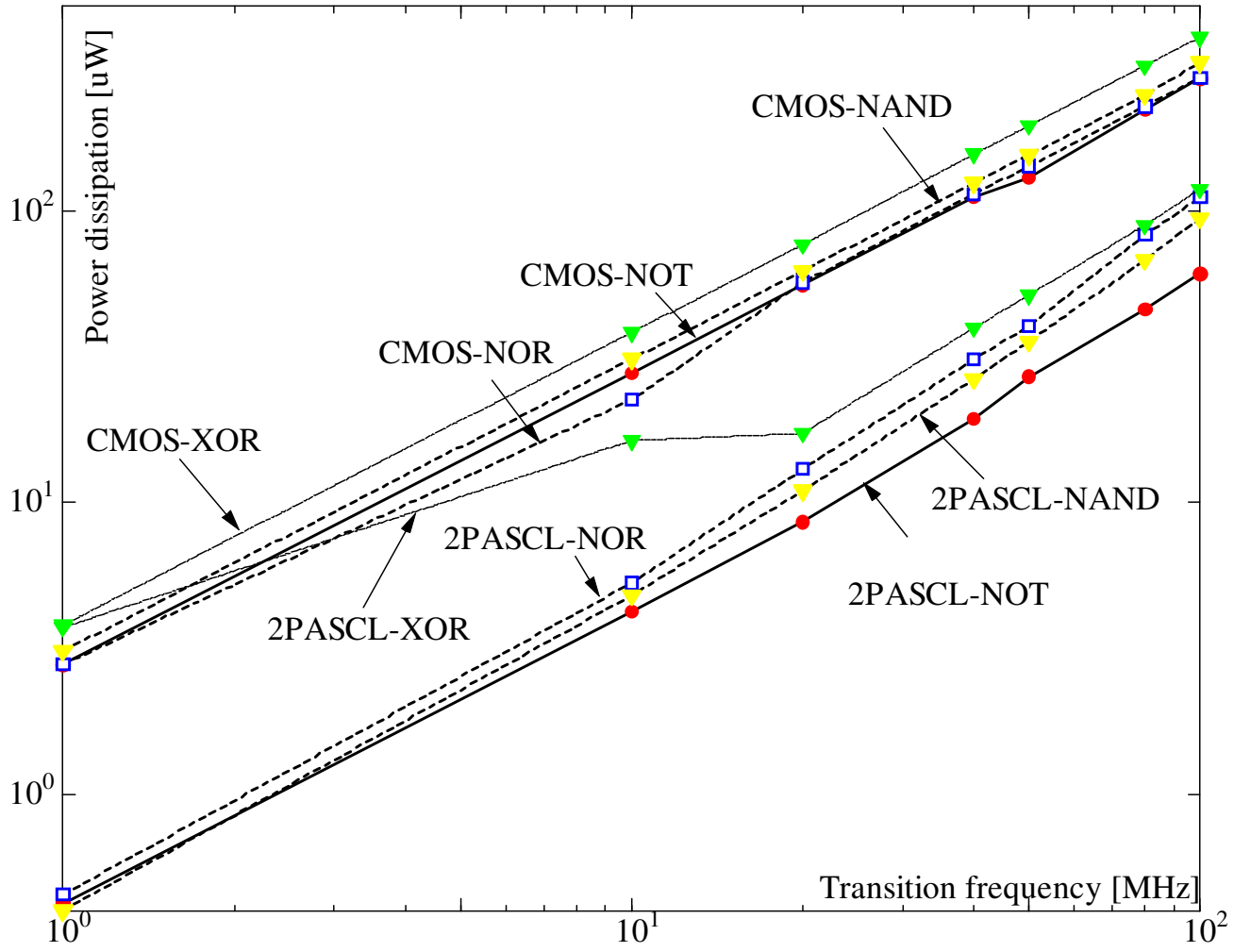

Fig. 8 Power dissipation comparison graph of 2PASCL and CMOS logics using 1.2μm process for f_T of 1 to 100 MHz.