Chain inverter and NAND logic comparison of 2PASCL and 2PADCL

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Abstract

The paper compares the SPICE simulations results on NOT and NAND logics of 2PASCL and 2PADCL. Then, the maximum possible number of inverters at different transition frequencies of both circuits are evaluated.

1 Introduction

Earlier, we have seen a significant power dissipation in 2PASCL NOT gates compared to CMOS and 2PADCL. From previous study, the clock frequency which is 2 times (2X) the transition frequency shows the lowest energy dissipation compared to 4X, 6X, 8X and 10X. We also found that 8-inverter chain of 2PASCL demonstrates 37% lower energy dissipation compared to CMOS 8-inverter chain. However, we are still yet to confirm on how many inverters can be possibly chained at different transition frequency for 2PASCL.

In this study, we simulate 2PASCL and 2PADCL NOT and NAND logics. Then we continue by evaluating their chain-inverter circuits. By changing the transition frequencies from 5 to 100 MHz, we examine the maximum number of inverter that can be chained. The output waveforms response must be within the evaluation phase for the inverter to be counted as valid.

2 2PASCL and 2PADCL comparison

2.1 NOT gate

NOT logic diagram using 2PASCL and 2PADCL topologies are as shown in Fig. 1. The output waveforms results are as demonstrated in Fig. 2. From the power dissipation result per cycle from the simulation, we plotted a comparison graph as in Fig. 3

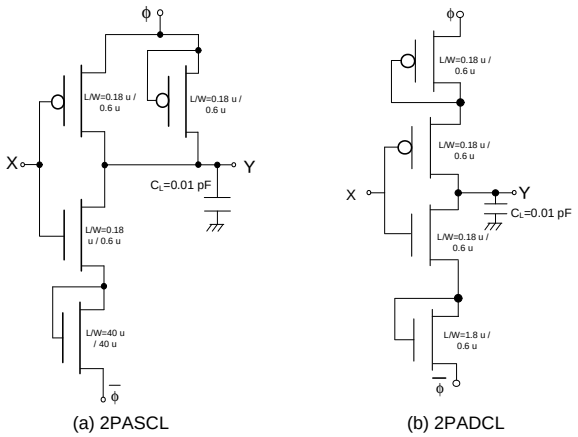

Fig. 1 Circuit diagram of (a)2PASCL NOT and (b) 2PADCL NOT.

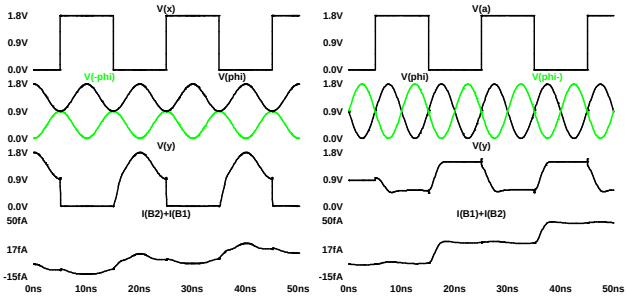

Fig. 2 Output waveforms of 2PASCL (left) and 2PADCL (right) at 50 MHz transition frequency.

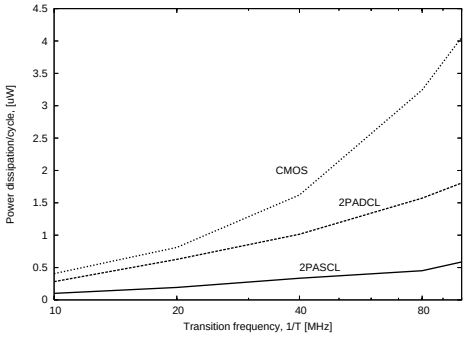

Fig. 3 Power dissipation comparison for 2PASCL, 2PADCL, and CMOS NOT logics when transition frequency is changed from 10 to 100 MHz.

2.2 NAND logic

Next, we evaluate the NAND logic of 2PADCL and 2PASCL which schematics are as shown in Fig. 4. The output waveforms are shown in Fig. 5

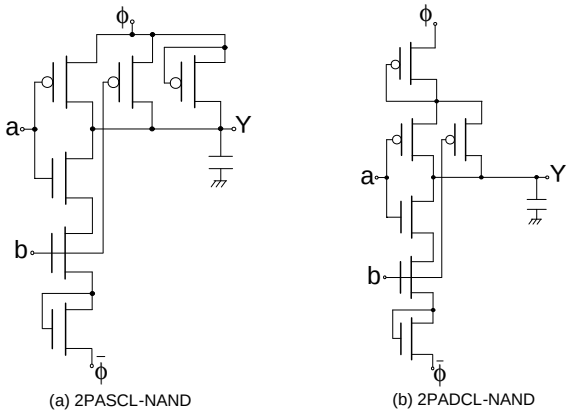

Fig. 4 Schematic for NAND logic for (a) 2PASCL and (b) 2PADCL.

We then compared the power dissipation of both topologies as presented in Fig. 6

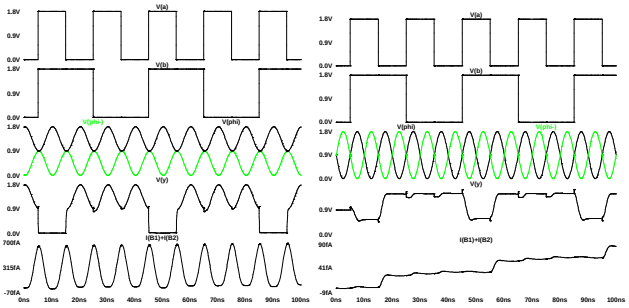

Fig. 5 Output waveforms of 2PASCL NAND (left) and 2PADCL NAND (right) at 50 MHz transition frequency.

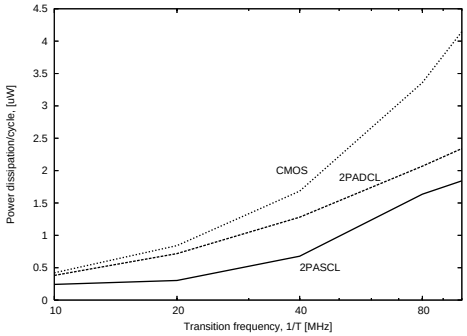

Fig. 6 Power dissipation comparison for 2PASCL, 2PADCL, and CMOS NAND logics when transition frequency is changed from 10 to 100 MHz.

3 Chain inverter comparison

Next, we evaluate the chain inverter and compare the results of 2PASCL and 2PADCL. For this simulation the valid inverter logic is when the output response is within the evaluation phase. From the evaluation and simulation, the results are as shown in Fig. 9

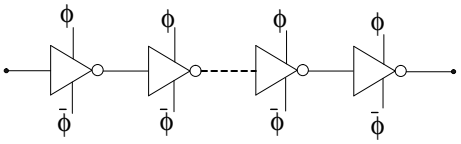

Fig. 7 Chain-inverter.

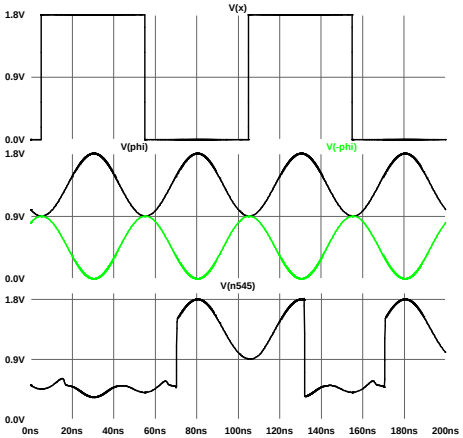

Fig. 8 Output waveforms for 358th inverter of 2PASCL.

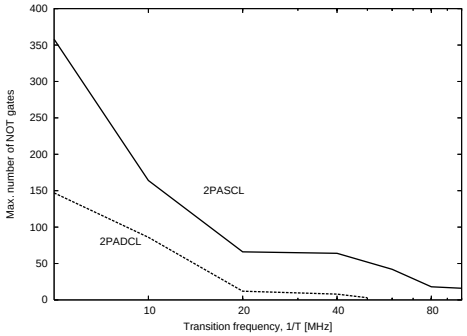

Fig. 9 Maximum number of NOT logics at 5 to 10 MHz transition frequencies.

4 Conclusion

From the results, 2PASCL shows the lower power dissipation than 2PADCL for NOT and NAND logics. From the chain inverter simulation results, we have also seen a significantly longer chain inverter can be connected using 2PASCL compared to 2PADCL.