A comparison of NOT, NAND and NOR of 2PASCL and 2PADCL

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Abstract

The paper compares the SPICE simulations results on NOT, NAND and, NOR logic gates of 2PASCL and 2PADCL. The results again show a lower power dissipation of all 2PASCL topologies gates. Finally, the layout design of 2PASCL NOT circuit is presented.

1 Introduction

Earlier, we have seen lower power dissipation of NOT and NAND logic gates of 2PASCL compared to 2PADCL. We also confirmed that significant longer chain inverter of 2PASCL is possible compared to 2PADCL. However for 2PASCL NAND circuit, we found an unstable energy dissipation (shown in the graph) which is a sine wave like shape. For 2PADCL, it is a step-like shape for the energy dissipation graph.

In this study, we continue the SPICE simulation after reinput the AD,AS,PD and PS for all the MOS transistors. Then we measure the energy dissipation of NOT, NAND and NOR circuit for both topologies. We also extend the symmetrical clock circuit shape of 2PASCL to overlapped and separated waveforms to see the difference in the power dissipation. Lastly we draft the first layout design of 2PASCL NOT circuit using 0.12 μm CMOS technology.

2 2PASCL and 2PADCL comparison

2.1 NOT gate

NOT logic schematic using 2PASCL and 2PADCL topologies are as shown in Fig. 1. The width (W) and length (L) are also shown in the schematic. The output waveforms results are as demonstrated in Fig. 3. From the power dissipation result per cycle from the simulation, we plotted a comparison graph as in Fig. 4. We also demonstrated the ovelapped and separated sinusoidal power clocks simulation results. For the overlapped power clocks, the amplitude is 1.1 V each clock. For the separated ones, the amplitude is 0.7 V each. From the comparison graph, we find that the overlapped clocks of 2PASCL shows a lower power dissipation compared to 2PASCL with non-overlapped clocks.

2.2 NAND logic gate

Next, we evaluate the NAND logic of 2PADCL and 2PASCL which schematics are as shown in Fig. 5. The output waveforms are shown in Fig. 6

We then compared the power dissipation of both topologies as presented in Fig. 7. For 1 MHz transition frequency, the result shows that 2PASCL NAND dissipates higher power compared to CMOS. This phenomenon need a further clarification.

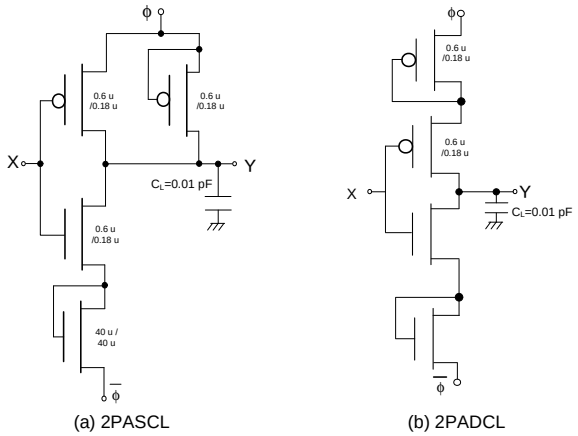

Fig. 1 Circuit diagram of (a)2PASCL NOT and (b) 2PADCL NOT.

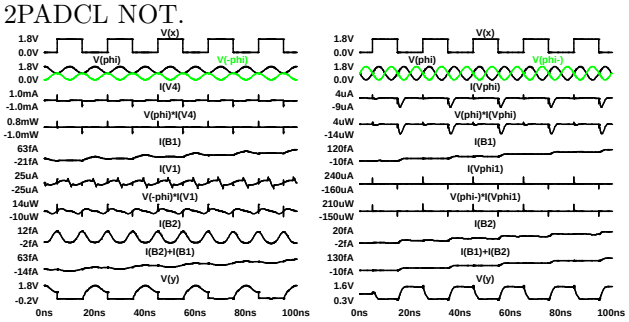

Fig. 2 Output waveforms of 2PASCL (left) and 2PADCL (right) at 50 MHz transition frequency.

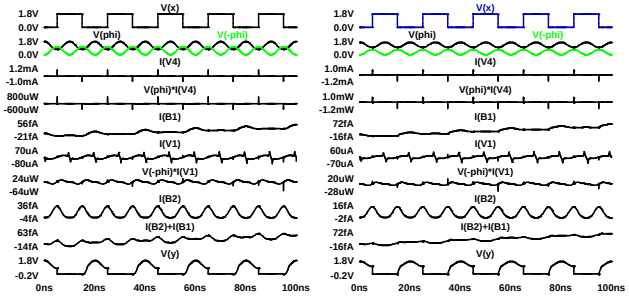

Fig. 3 Output waveforms of overlapped clocks of 2PASCL (left) and separated clocks of 2PASCL (right) at 50 MHz transition frequency.

2.3 NOR logic gate

Next, we evaluate the NOR logic of 2PADCL and 2PASCL which schematics are as shown in Fig. 5. The output waveforms are shown in Fig. 8. We can see at almost all the transition frequency from 1 to 100 MHz, 2PASCL NOR logic shows the lowest in power dissipation.

We then compared the power dissipation of both topologies as presented in Fig. 10

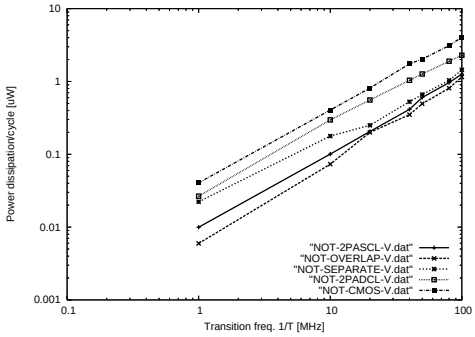

Fig. 4 Power dissipation comparison for 2PASCL, overlapped and separated clocks of 2PASCL, 2PADCL, and CMOS NOT logics when transition frequency is changed from 10 to 100 MHz.

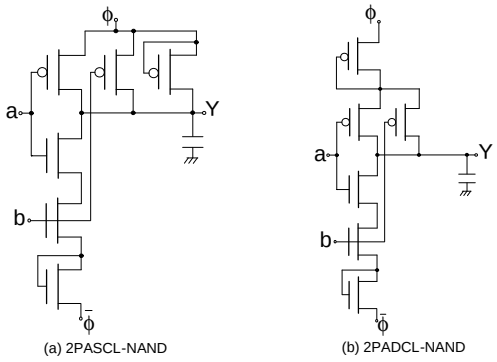

Fig. 5 Schematic for NAND logic for (a) 2PASCL and (b) 2PADCL.

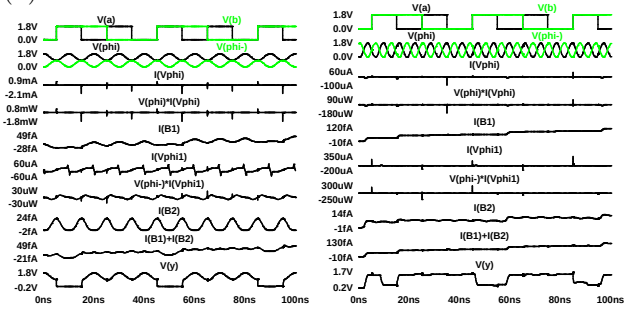

Fig. 6 Output waveforms of 2PASCL NAND (left) and 2PADCL NAND (right) at 50 MHz transition frequency.

3 2PASCL inverter layout design

By using the layout editor of L-Edit (ver. 12.11) from Tanner EDA, we draft the 2PASCL NOT logic. As described in the following design draft, the components are divided into well, contact, active, via, 1 AL, P+ and 1 Poly. For this fist design, the author needs a little more time to get use before can design a good layout.

4 Conclusion

From the results, 2PASCL generally shows the lower power dissipation than 2PADCL for NOT, NAND and NOR logics. We also find that the overlapped power clocks with the amplitude of 1.1 V each shows lower than the non-overlapped clocks.

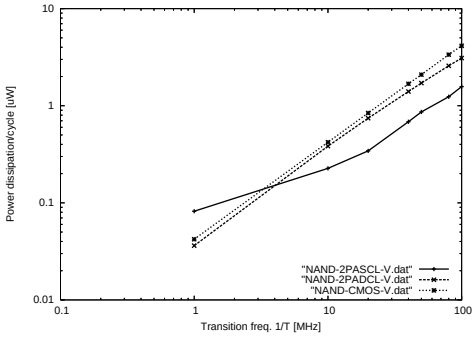

Fig. 7 Power dissipation comparison for 2PASCL, 2PADCL, and CMOS NAND logics when transition frequency is changed from 10 to 100 MHz.

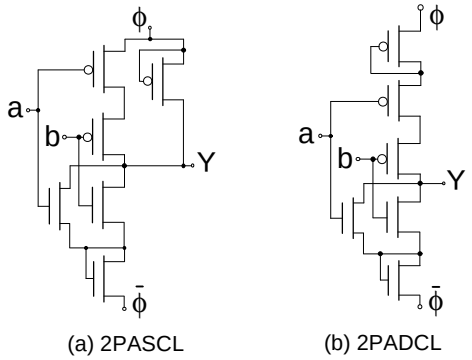

Fig. 8 Schematic for NAND logic for (a) 2PASCL and (b) 2PADCL.

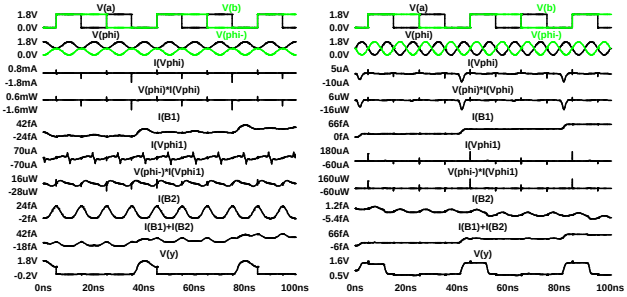

Fig. 9 Output waveforms of 2PASCL NOR (left) and 2PADCL NOR (right) at 50 MHz transition frequency.

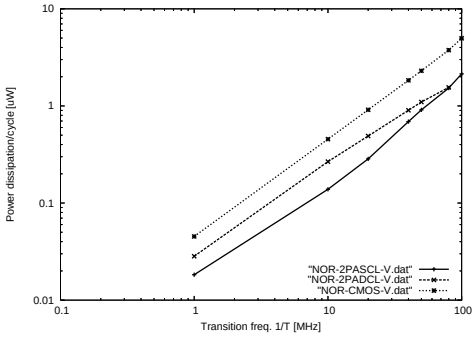

Fig. 10 Power dissipation comparison for 2PASCL, 2PADCL, and CMOS NAND logics when transition frequency is changed from 10 to 100 MHz.