Overlapped power voltage and low V_{dd} evaluation

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Abstract

The paper proposes the best condition of overlapped power voltage supply comparing the power dissipation of each conbinations. Then, the peak clock voltage is reduce and simulation at 1.2V and 0.8 V are compared. We also present the theory of the low energy dissipation in 2PASCL by explaning the junction capacitance of pMOS diode.

1 Introduction

Earlier, from the results, 2PASCL generally shows lower power dissipation than 2PADCL for NOT, NAND and NOR logics. We also find that the overlapped power clocks with the amplitude of 1.1 V each shows lower than the non-overlapped clocks.

In this study, we evaluate the best ratio of overlapped power clocks. Then, by reducing the peak voltage of the clock, we examine the lowest voltage where the circuit still operated using 0.18 μm CTX CMOS process SPICE simulation. We also show the theory of junction capacitance of pMOS diode in 2PASCL where the charges are stored and total energy dissipation is reduced. Lastly, correction of earlier layout design of 2PASCL NOT circuit using 0.12 μm CMOS technology is carried out.

2 Best conditions of 2PASCL to reduce power dissipation

2.1 Overlapped power clocks evaluation

Table 1 The combination of power clock voltage done in this study. The height of the peak for the clock is 1.8V. The input frequency is 50 MHz.

Amplitude of ϕ [V]/ $\overline{\phi}$ [V]	Diff. [V]	Diss. [uW]
0.7/0.7	-0.4	0.831
0.75/0.75	-0.3	0.767
0.8/0.8	-0.2	0.682
0.85/0.85	-0.1	0.629
0.9/0.9	0	0.583
0.95/0.95	0.1	0.542
1.0/1.0	0.2	0.519
1.05/1.05	0.3	0.535
1.1/1.1	0.4	0.535
1.15/1.15	0.5	0.576
1.21/1.2	0.6	0.619

The results are as demonstrated as a graph in Fig. 1. From the power dissipation result per cycle from the simulation, we understand that with the gap of 0.2 overlapped between each peaks, it shows the lowest in energy dissipation.

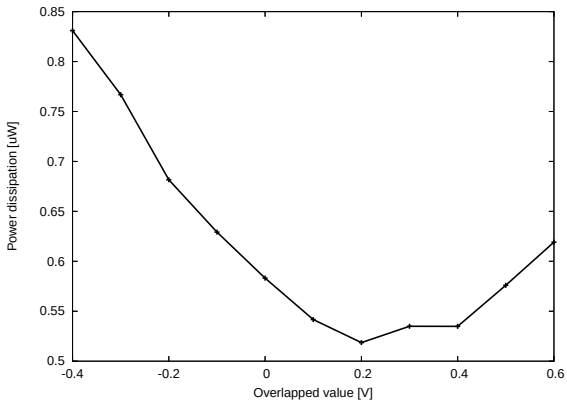

Fig. 1 Overlapped power clocks comparison graph.

2.2 Low height of power clock evaluation

Next, by reducing the peak voltage of the power clock we compared the power dissipation of CMOS and 2PASCL. This evaluation is to find the minimum operated voltage clock with 0.18 μm CTX CMOS process. The results are as shown in Fig. 2.

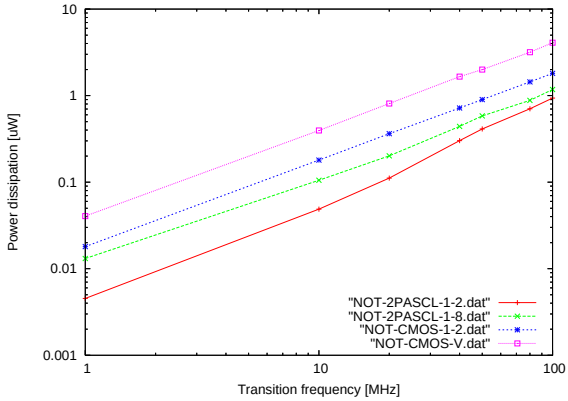

Fig. 2 Comparison of power dissipation of 2PASCL and CMOS NOT logics at different peak clock voltage or V_{dd}.

Then to further evaluate this, we examine both circuits at 0.8 V. Both circuits are functioning correctly. From the simulation results, we found that the threshold voltage of nMOS, V_{tn} is 0.58 V and for pMOS, V_{tp} is -0.24 V.

3 Junction capacitance of pMOS diode

In this paper we also has another theory of the low energy dissipation of 2PASCL compared to other adi-

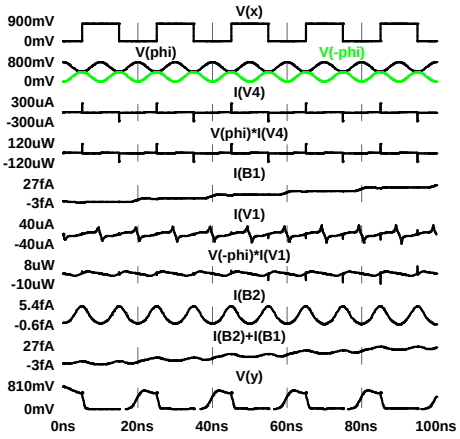

Fig. 3 Output waveforms of 2PASCL NOT logic at 50 MHz transition frequency and peak voltage clock at 0.8V.

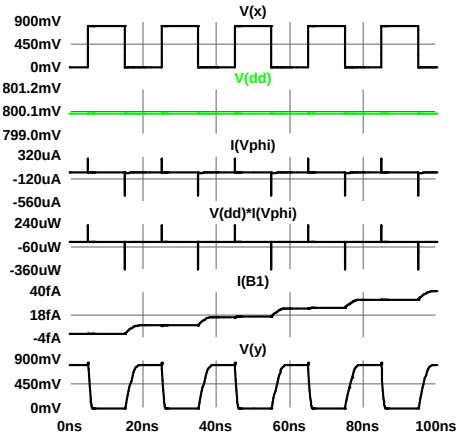

Fig. 4 Output waveforms of CMOS NOT logic when Vdd is 0.8V at 50 MHz transition frequency.

abatic logics. As the + and - currents flow frequently through the on-resistance and pMOS diodes as demonstrated in the output waveforms, we found that pMOS diodes in 2PASCL worked as the junction capacitance where charges are stored without any energy dissipation occurs. The equivalent circuit of 2PASCL including the diodes are as explain in Fig. 5.

4 2PASCL inverter layout design

Correction of 2PASCL inverter layout design has been done. The corrections are the contacts for the gates, the schematic of poly according to design rules and merging of the metal contacts. This design has been gone through DRC and passed accrodingly.

5 Conclusion

From the results, overlapped power clocks can be used and we found that 0.2 gap between peak and peak during overlapping shows the lowest power dissipation. And for this technology a reduction to 0.8 V still shows that circuit are functioning correctly at 50 MHz transition frequency.

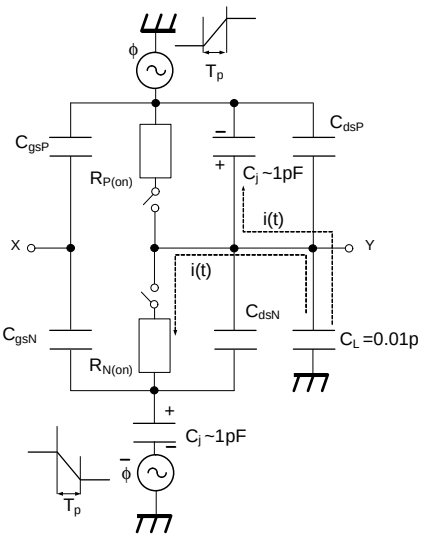

Fig. 5 Equivalent circuit for 2PASCL.