Preliminary study on 4x4 array multiplier and plans for 2010

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Abstract

The paper presents a preliminary study on 4x4 array multiplier and the plan for year 2010 for 2PASCL circuits.

1 4x4 array multiplier

In this paper, preliminary study on the 4x4 bit array multiplier has been studied. 4x4 bit array multiplier consist of half adders and full adders as shown in Fig. 4.

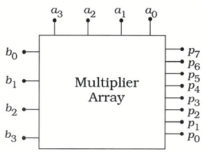

Fig. 1 An array multiplier.

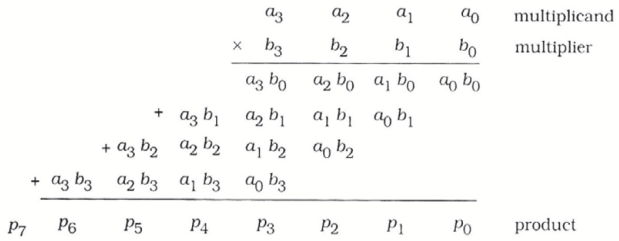

Fig. 2 Multiplication of two 4-bit words.

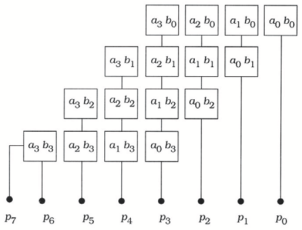

Fig. 3 Modulized view of the multiplication sequence.

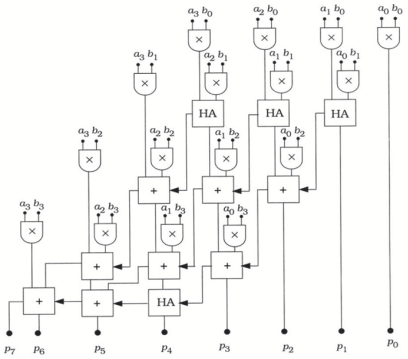

Fig. 4 Details for a 4x4 array multiplier.

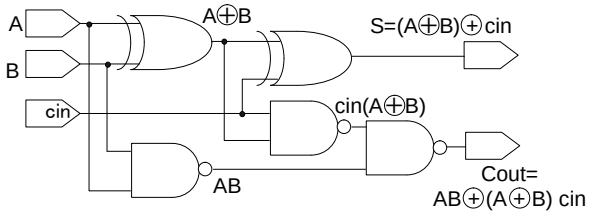

Fig. 5 Full adder which consist of XOR and NAND logics.

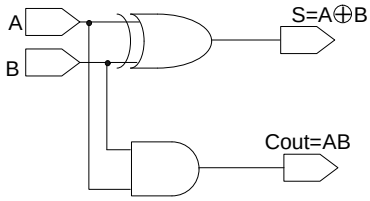

Fig. 6 Half adder which consist of XOR and AND logic.

2 Plans for year 2010

2.1 4x4 bit array multiplier simulation and layout design

2.2 Paper with the title of "Overlapped sinusoidal split level voltage clock evaluation for low-power 2PASCL circuit" for IEICE 2010 in Sendai

2.3 Begin studies on FPGA

2.4 Additional work: Hands-on on EPSON microcontroller module