SPICE simulation on 2PASCL 4x4 bit array multiplier

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Abstract

The paper presents a SPICE simulation on 2PASCL 4x4 bit array multiplier.

1 4x4 array multiplier

1.1 Simulation and results

Previously, a preliminary study has been done on the 4x4 bit array multiplier as shown in Fig. 1 and Fig. 2. After considering the type of combination circuit for half adders and full adders as shown in Fig. 3 and Fig. 4, we simulate a full 2PASCL 4x4 bit array multiplier using 0.18 μm standard CMOS process. The 4x4 bit array multipler simulated in this paper are using 4 half adders, 8 full adders, 16 NANDs and 16 NOT circuits. All are using 2PASCL topologies. The block diagram of 4x4 bit array 2PASCL multiplier is demonstrated in Fig. 5, which is taken from SPICE simulation circuit diagram. The simulation results for 1 MHz transition frequency at are as shown in Fig. 6. The result for $(1111)_2$ x $(1111)_2$ = $(11100001)_2$ is used to check the result.

$$
\begin{array}{rccccccl}
 & & & a_3 & a_2 & a_1 & a_0 & \text{multiplicand} \\
 & & \times & b_3 & b_2 & b_1 & b_0 & \text{multiplier} \\
\hline
 & & & a_3\,b_0 & a_2\,b_0 & a_1\,b_0 & a_0\,b_0 & \\
 & & + & a_3\,b_1 & a_2\,b_1 & a_1\,b_1 & a_0\,b_1 & \\
 & & + & a_3\,b_2 & a_2\,b_2 & a_1\,b_2 & a_0\,b_2 & \\
 & + & a_3\,b_3 & a_2\,b_3 & a_1\,b_3 & a_0\,b_3 & & \\
\hline
p_7 & p_6 & p_5 & p_4 & p_3 & p_2 & p_1 & p_0 \quad \text{product}
\end{array}
$$

Fig. 1 Multiplication of two 4-bit words.

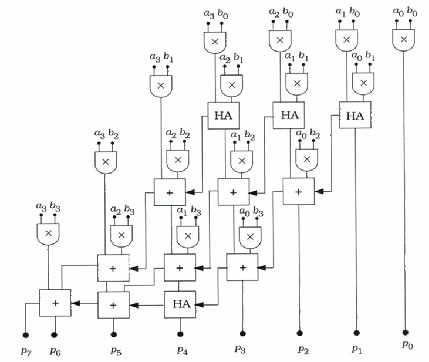

Fig. 2 Details for a 4x4 array multiplier.

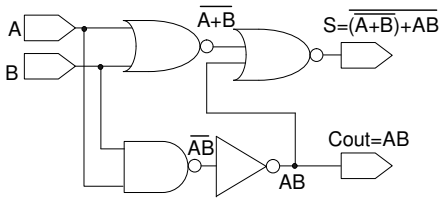

Fig. 3 Half adder which consist of NOR, NAND and NOT logic.

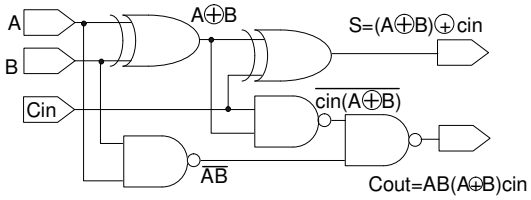

Fig. 4 Full adder which consist of XOR and NAND logics.

2 Conclusion

From the simulation results, 4x4 bit array 2PASCL at 1 MHz transition frequency shows that circuit is operated well. This proofs that the circuit diagram is correct. The output waveforms will be improved in the next simulation report. The next simulation will be the calculation of the energy and a comparison with 4x4 bit array CMOS multiplier.

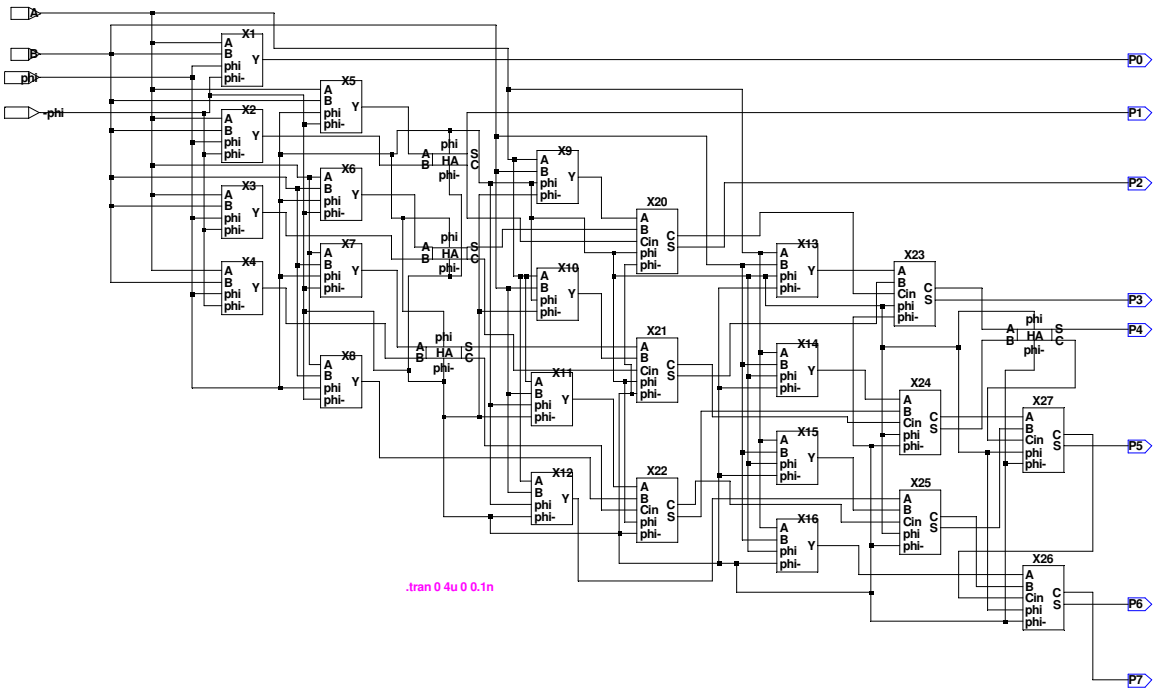

Fig. 5 4x4 array multiplier block diagram.

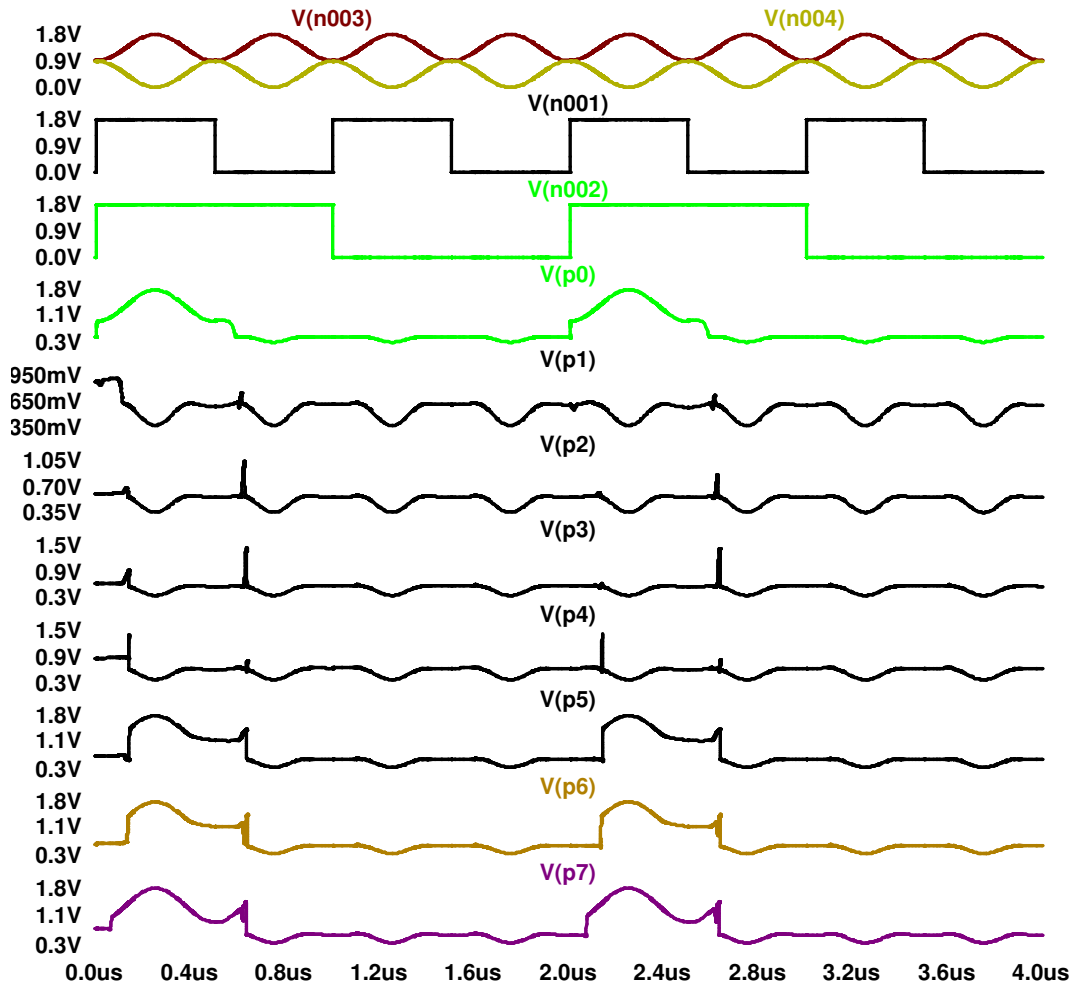

Fig. 6 Output waveforms.