4x4 bit array 2PASCL multiplier simulation : a power dissipation comparison with CMOS

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Abstract

The paper compares the simulation results of 4x4 bit array 2PASCL multiplier with that of CMOS.

1 4x4 array multiplier

1.1 Simulation and results

The details are shown in Table 1. Figure 1 shows the power dissipation comparison. From the graph, at 1 MHz transition frequency, f_T, the difference is 63%.

Table 1 Details of 4x4 bit array multiplier in the simulation.

Topology	2PASCL and CMOS
L/W	0.18 μm / 0.6 μm
No. of logics	4 HA, 8 FA, 16 AND
Inputs	a_0,a_1,a_2,a_3,b_0,b_1,b_2,b_3
Outputs	p_0,p_1,p_2,p_3,p_4,p_5,p_6,p_7

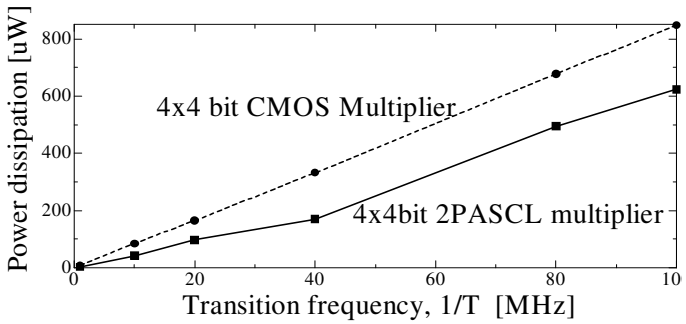

Fig. 1 Power dissipation comparison.

2 Conclusion

4x4 bit array multiplier using 2PASCL has been carried out. From the simulation results, at more than 50 MHz transition frequency, the output waveforms degradation occurs. However, the power dissipation is 63% lower than that of CMOS.

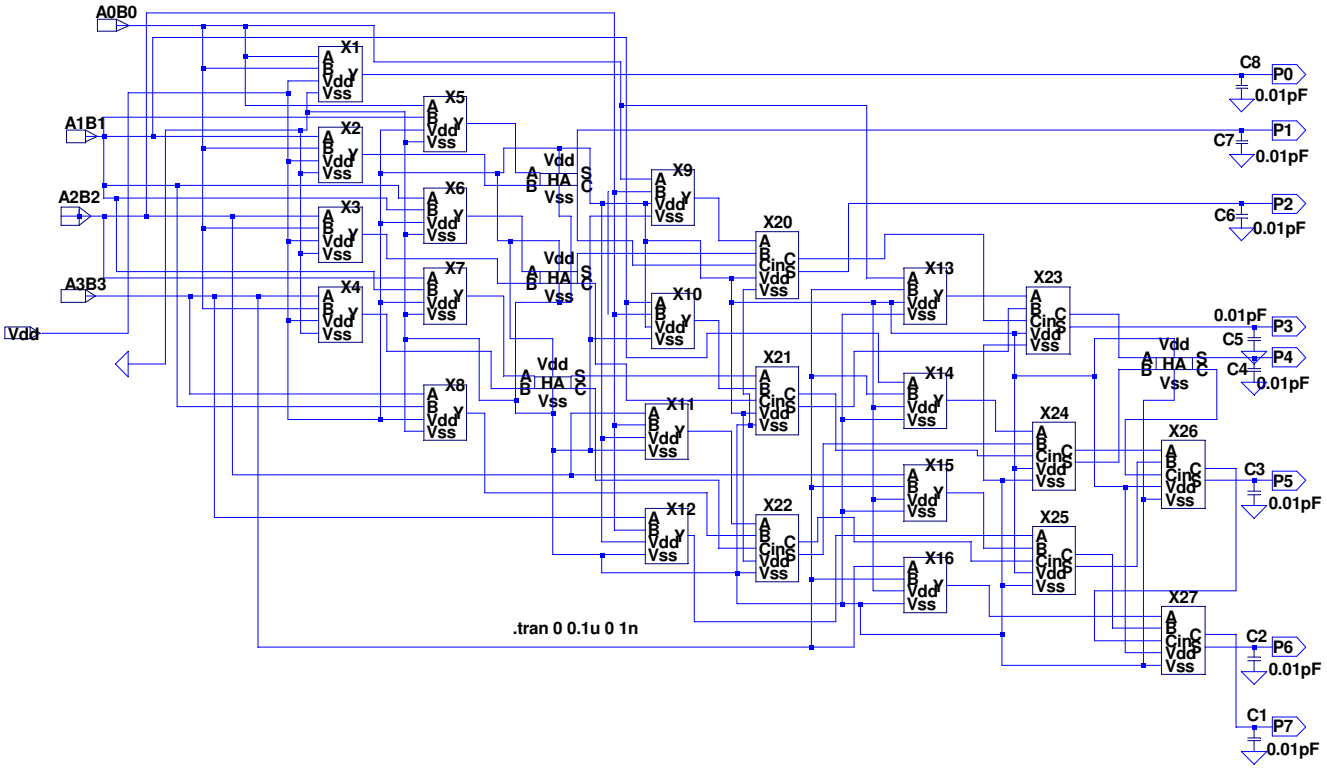

Fig. 2 4x4-bit array CMOS multiplier block diagram.

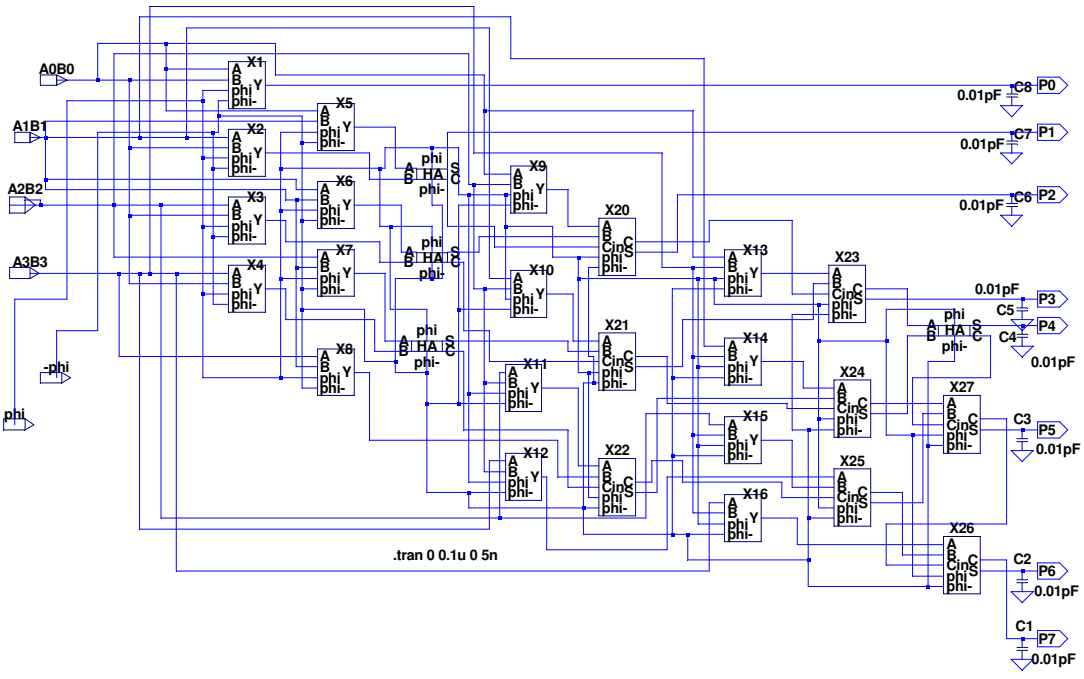

Fig. 3 4x4-bit array 2PASCL multiplier block diagram.

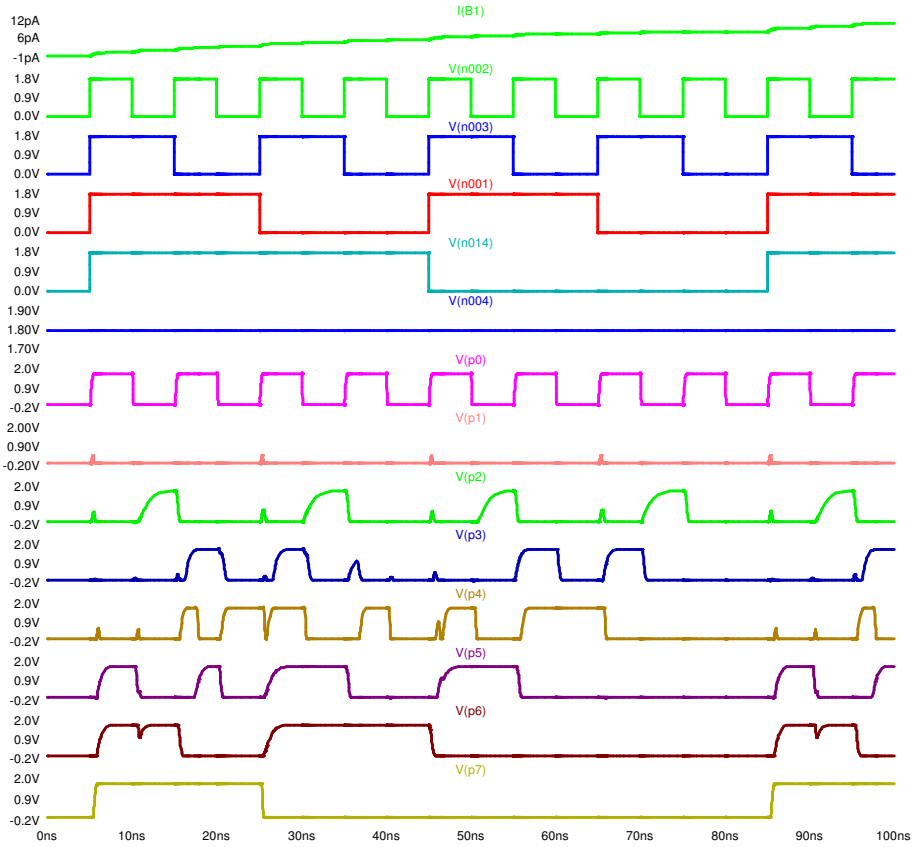

Fig. 4 Output waveforms of 4x4-bit array CMOS multiplier, f_T=100 MHz.

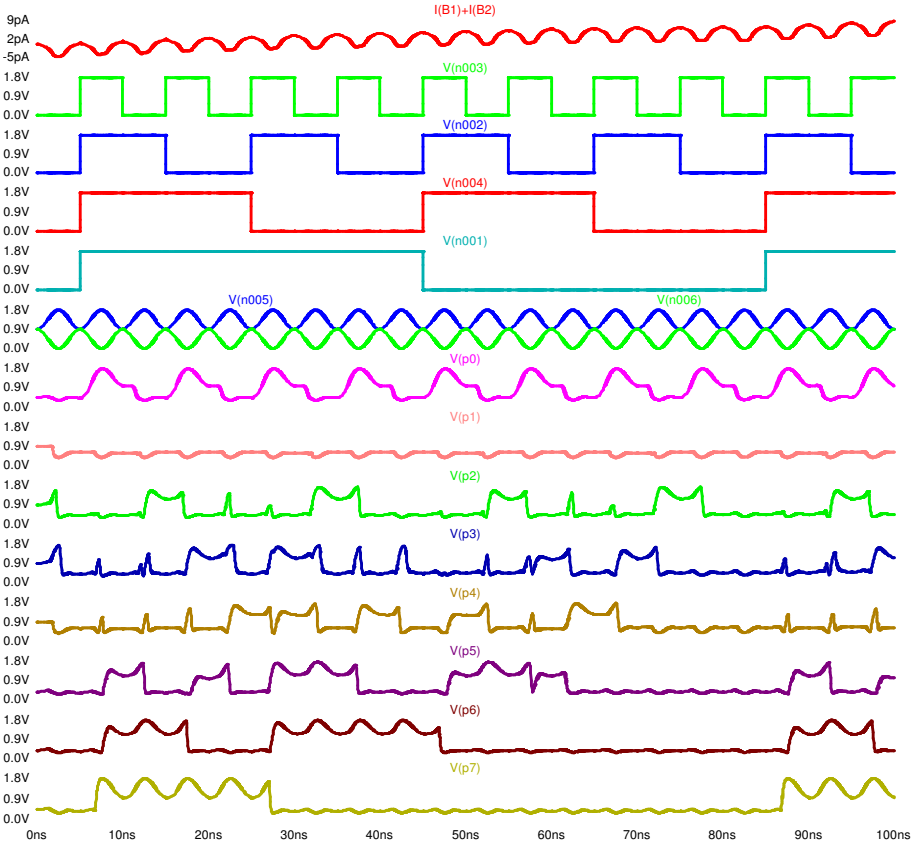

Fig. 5 Output waveforms of 4x4-bit 2PASCL multiplier at f_T=100 MHz.

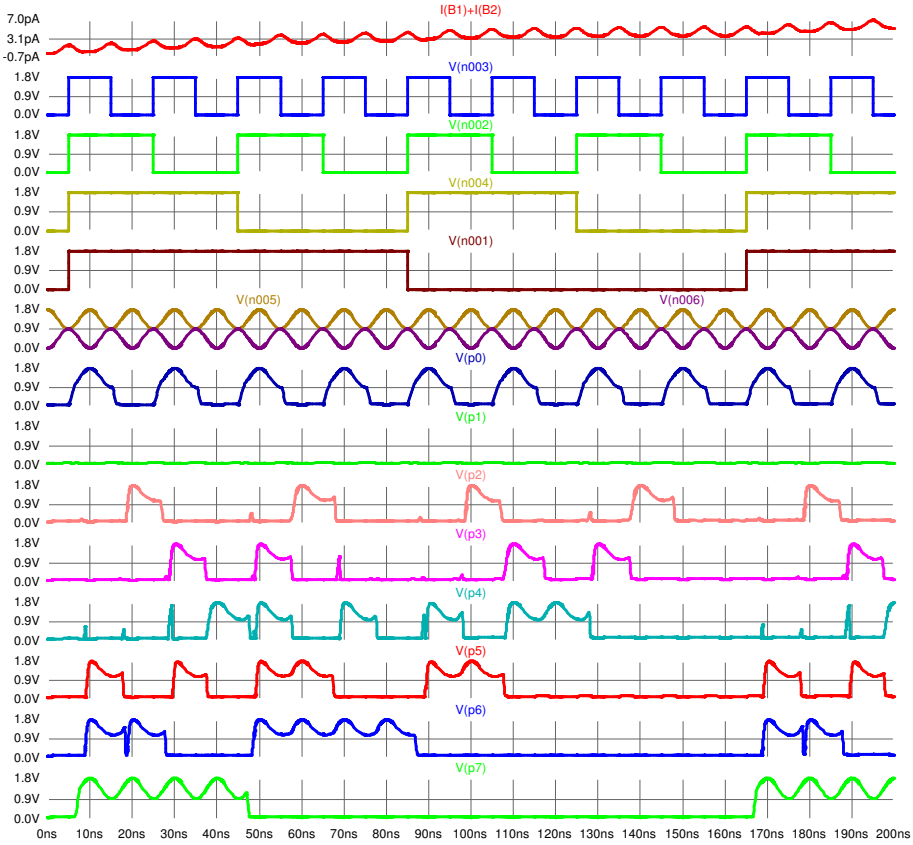

Fig. 6 Output waveforms of 4x4-bit 2PASCL multiplier at f_T=50 MHz.

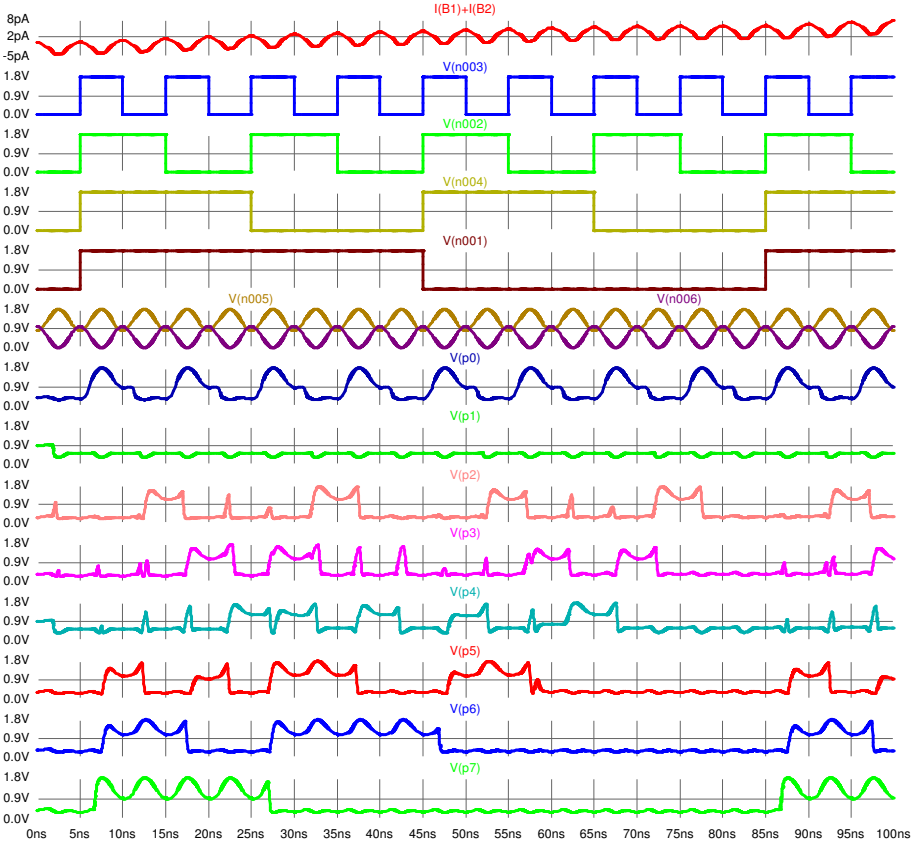

Fig. 7 Output waveforms of 4x4-bit 2PASCL multiplier with overlapped clocks at f_T=100 MHz. The power dissipation difference with non-overlapped is 9.5%

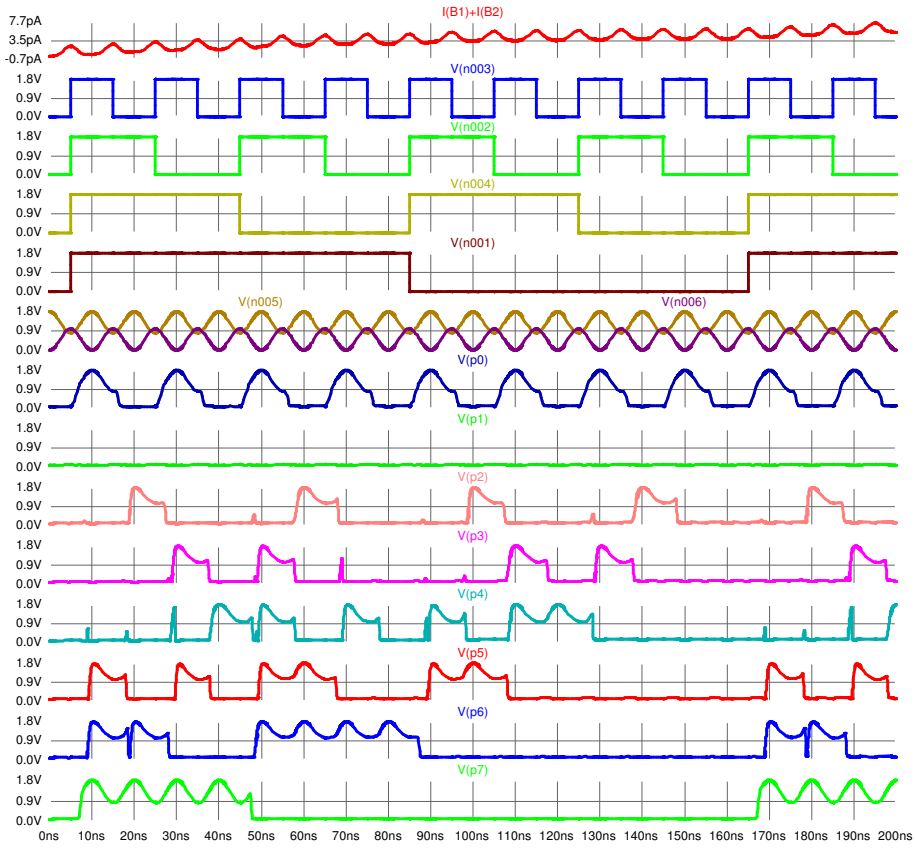

Fig. 8 Output waveforms of 4x4-bit 2PASCL multiplier with overlapped clocks at f_T=50 MHz.