4x4 bit array 2PASCL multiplier simulation and lay-out design

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Abstract

The paper demonstrate the simulation results of 4-bit 2PASCl multiplier. Lay-out designs of 2PASCL 2AND, 2XOR, 1-bit full adder, 1-bit half adder, D-flipflop and first draft of 2PASCL multiplier layout are also presented.

1 4x4 array multiplier

1.1 Simulation and results

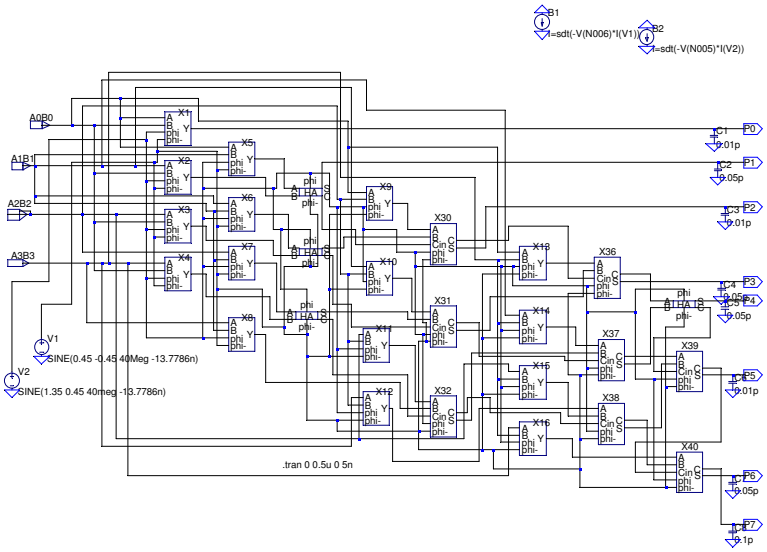

Fig. 1 LTSPice diagram of 4x4 bit 2PASCl Multiplier.

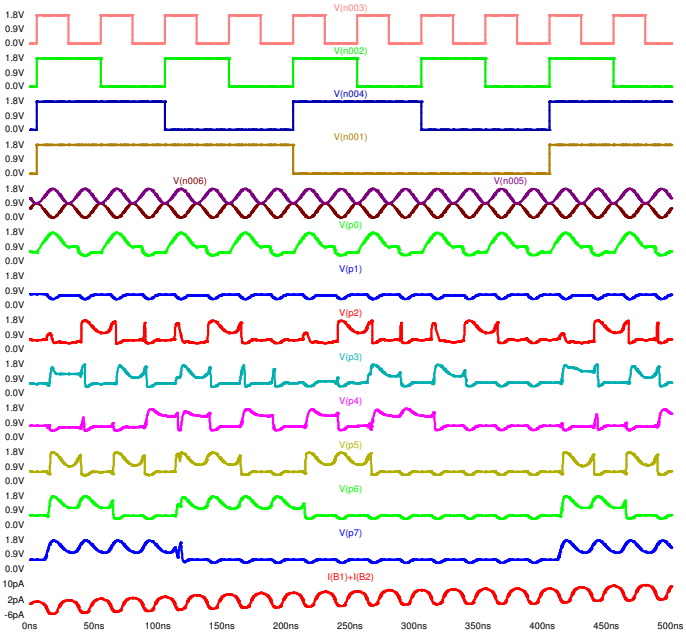

Fig. 2 Output waveforms of the diagram in Fig. 1.

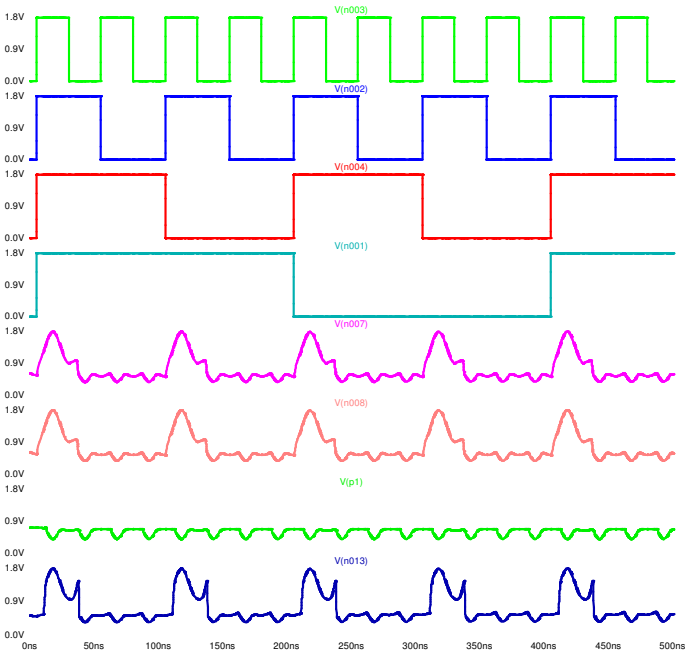

Fig. 3 Output waveforms of the half adder HA1.

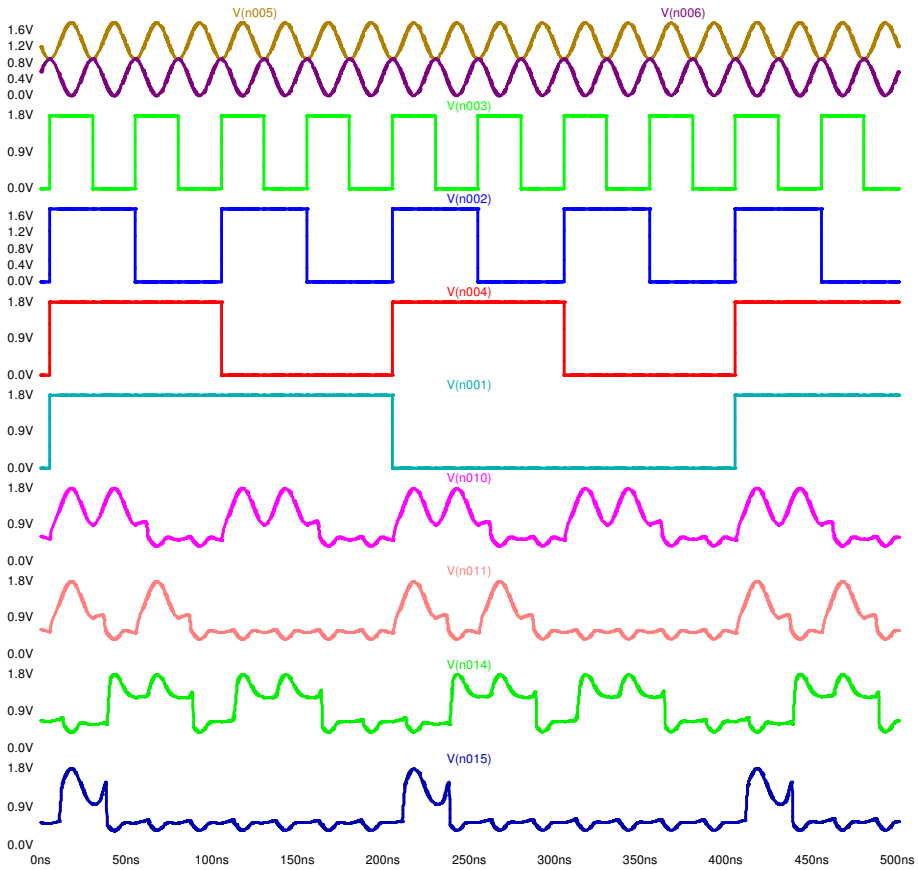

Fig. 4 Output waveforms of the half adder HA2.

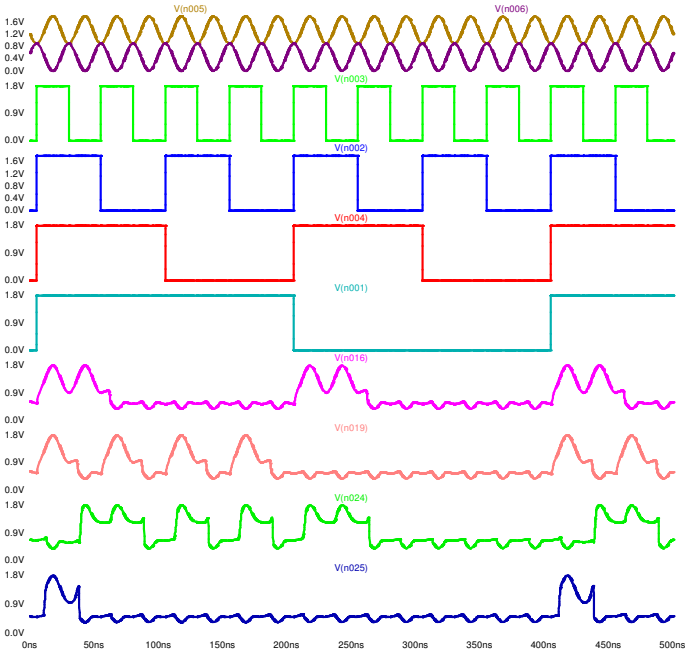

Fig. 5 Outpur waveforms of the half adder HA3.

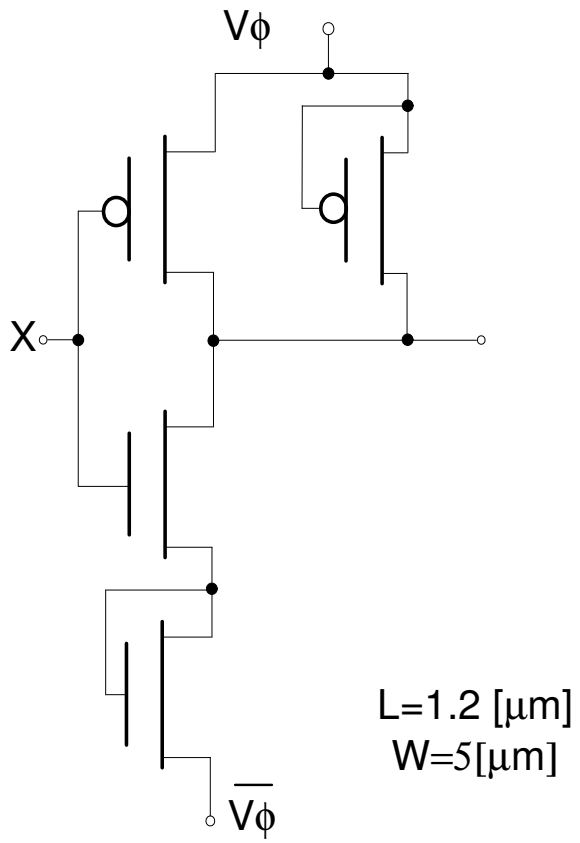

Fig. 6 Diagram for 2PASCL NOT.

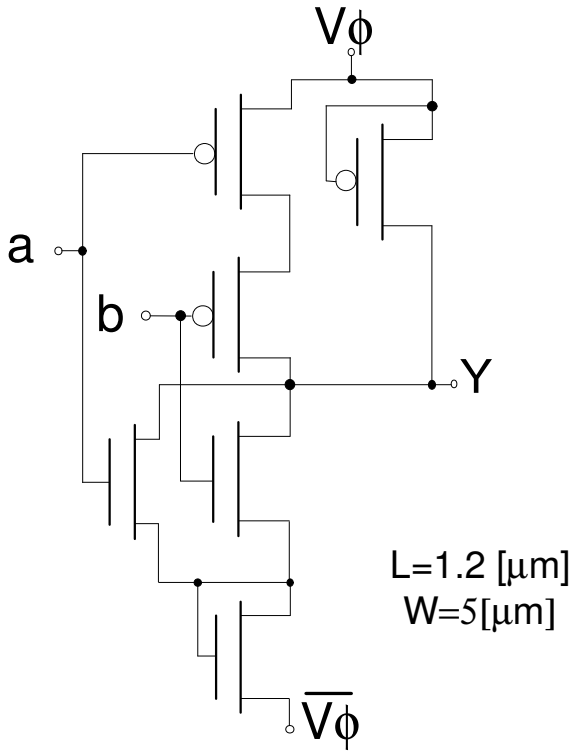

Fig. 7 Diagram for 2PASCL 2NOR.

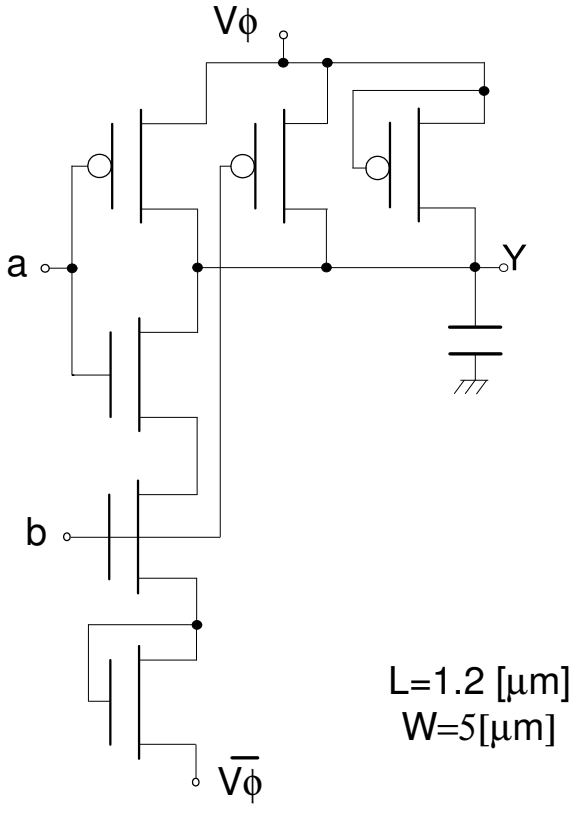

Fig. 8 Diagram for 2PASCL 2NAND.

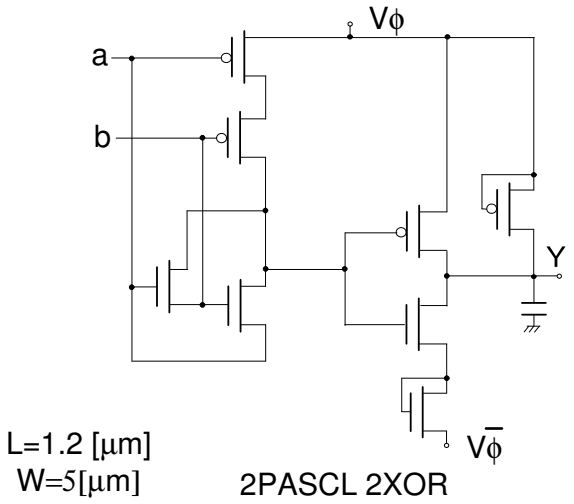

Fig. 9 Diagram for 2PASCL 2XOR.

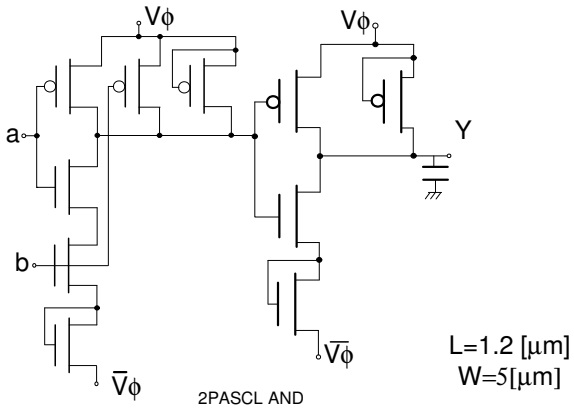

Fig. 10 Diagram for 2PASCL 2AND.

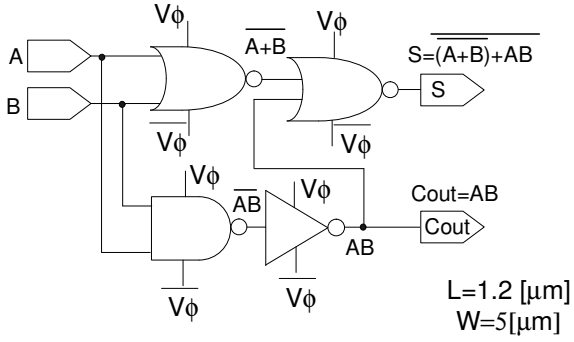

Fig. 11 Diagram for 2PASCL 1-bit Half adder.

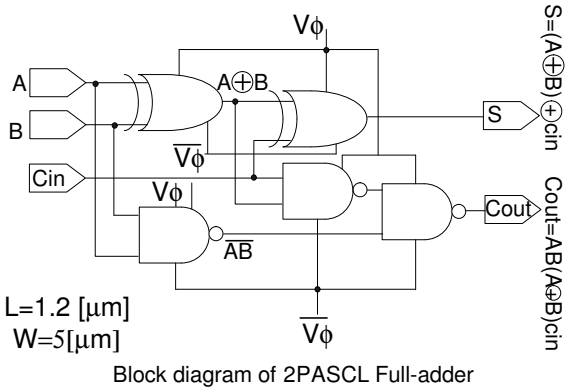

Fig. 12 Diagram for 2PASCL 1-bit Full adder.

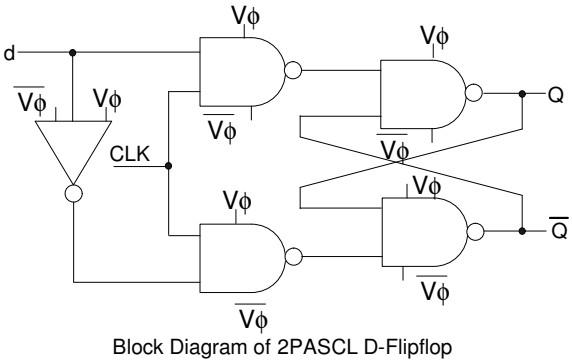

Fig. 13 Diagram for 2PASCL D-flipflop.

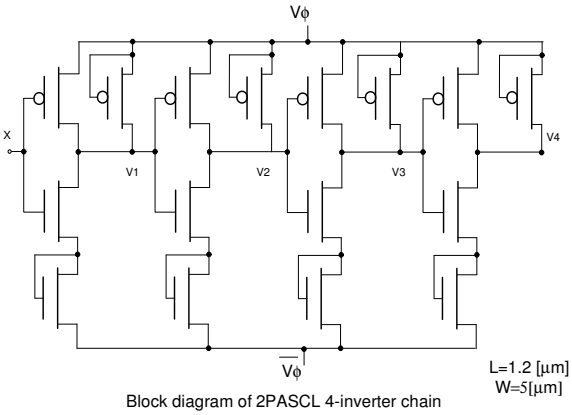

Fig. 14 Diagram for 2PASCL 4-inverter chain.

2 Conclusion

The SPICE simulation of 4x4 bit array multiplier using 2PASCL has been carried out for 20 MHz. The design lay-out of 2PASCL NOT, 2NAND and 2NOR has started. Next design will be XOR.