4×4-bit 2PASCL Multiplier Simulation using 1.2μm process : evaluation on high ripples at outputs

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Abstract

The paper demonstrate the simulation results of 4×4-bit 2PASCL multiplier using 1.2 μm process. A study on the effect of nMOS and pMOS diodes W and L to achieve a better low level of the signal is carried out. W/L of the logic transistors used in the simulations are 5.0μ/1.2 μ.

1 Introduction

We observed oscillations and high voltage of the signal 's low level logic. After changing the L values, not so significant improvements on the output signal seen. However, slight difference in the ripple values when we change the W values. In this paper we evaluate the W of 5.0,15.0 and 25.0μm. The L is remain at 1.2μm.

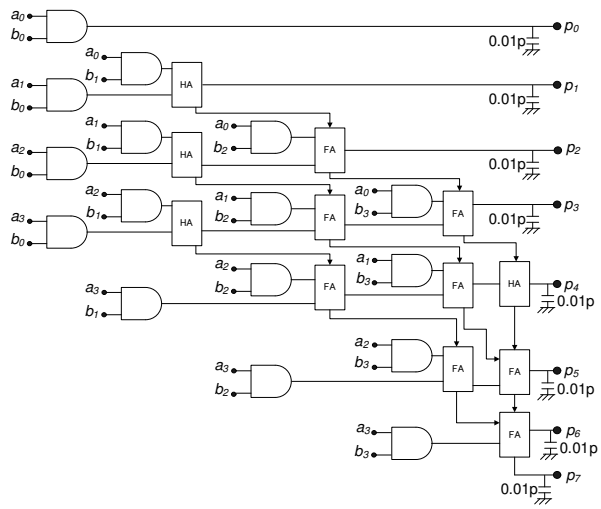

Fig. 1 Schematic of 4×4-bit 2PASCL multiplier showing the load capacitance at each output

2 Results

From Table 1, we found that for 4× 4-bit 2PASCL multiplier using 1.2 μm process, at 4 outputs i.e. p_1,p_2,p_3, and p_4, they show a very high ripple outputs. We will trace back the signal of the most severe p_3 from the simulation.

3 Conclusion

The SPICE simulation of 2PASCL logics using 1.2μ CMOS procees which leads to the fabrication has been carried to inspect the cause for the higher "0" signal level. From the results, we found that the ripple starts from the half adders. Further evaluation on the half adders will be done.

Table 1 Max of low level observed [V].

	W=5.0μ	W=15.0μ	W=25.0μ
p_0	0.87	0.83	0.81
p_1	1.96 (ripple)	1.80 (ripple)	1.70 (ripple)
p_2	2.94 (ripple)	2.41 (ripple)	3.29 (ripple)
p_3	3.27 (big ripple)	3.74 (big ripple)	4.66 (big ripple)
p_4	3.50 (ripple)	2.17 (ripple)	4.42 (big ripple)
p_5	0.92	0.79	0.90
p_6	0.98	0.81	0.76
p_7	1.00	0.83	0.80

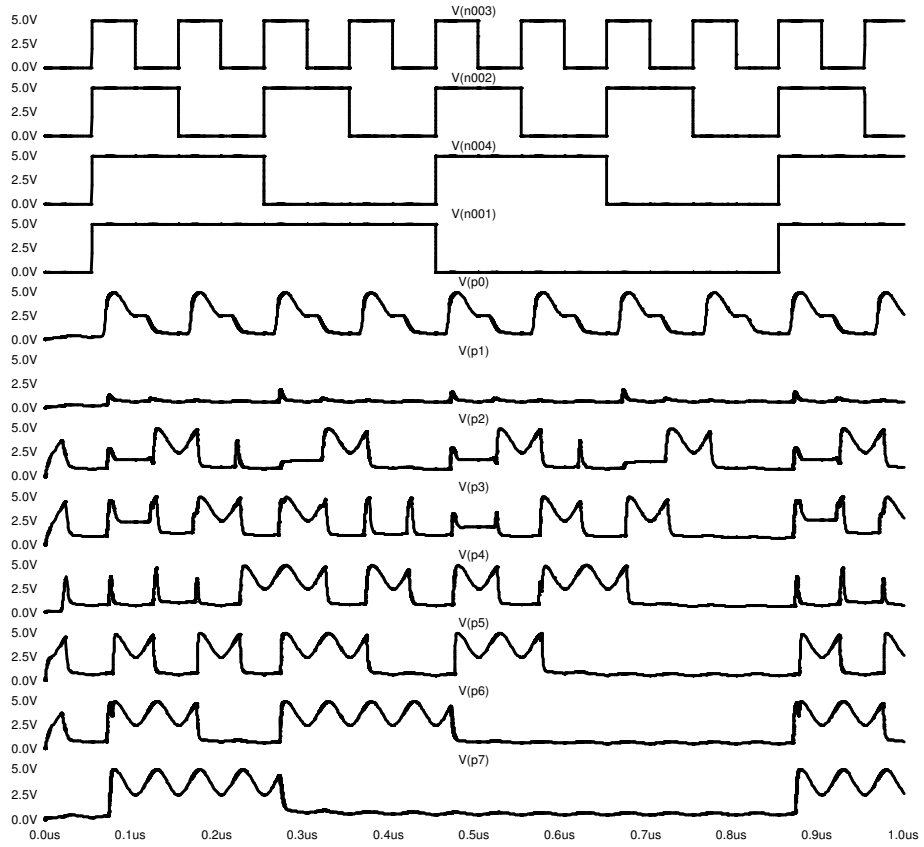

Fig. 2 4×4-bit 2PASCL multiplier at 10 MHz f_T using W=5.0μ.

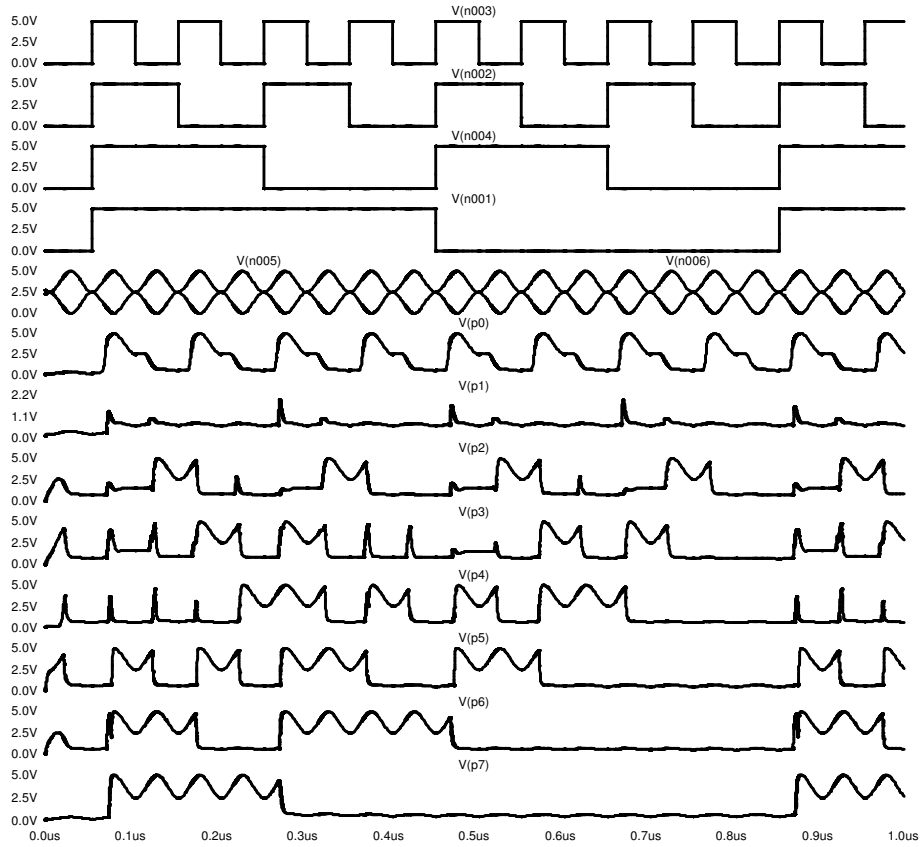

Fig. 3 4×4-bit 2PASCL multiplier at 10 MHz f_T using W=15.0μ.

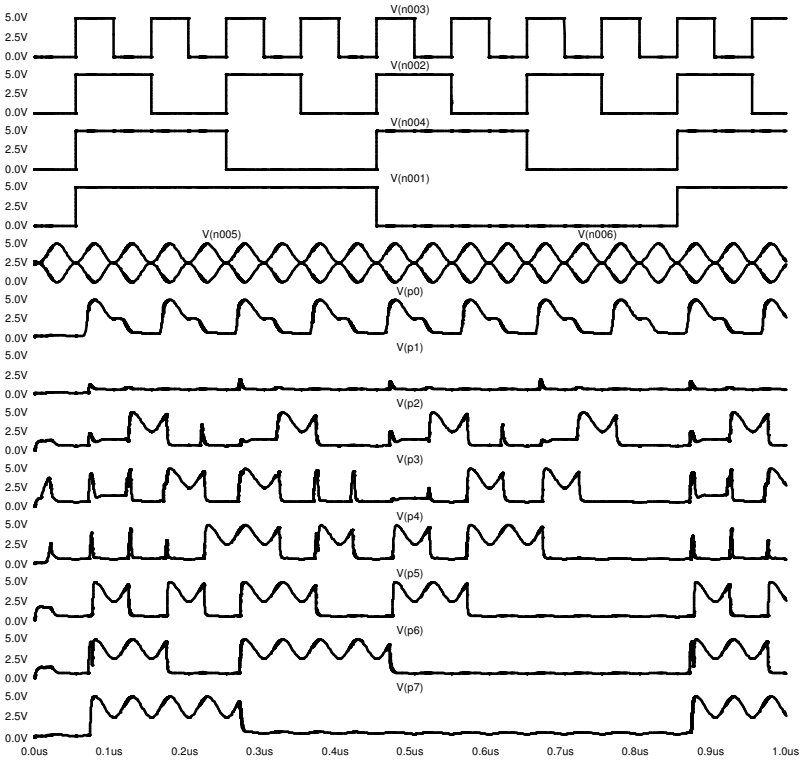

Fig. 4 4×4-bit 2PASCL multiplier at 10 MHz f_T using W=15.0μ.

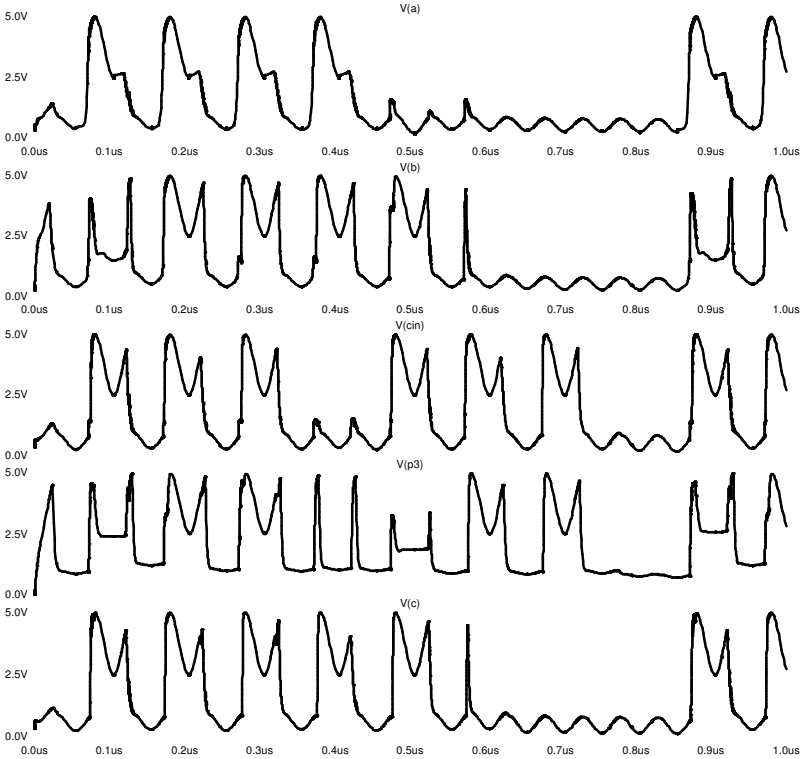

Fig. 5 4×4-bit 2PASCL multiplier at 10 MHz f_T using W=5.0μ at p_3 full adder.

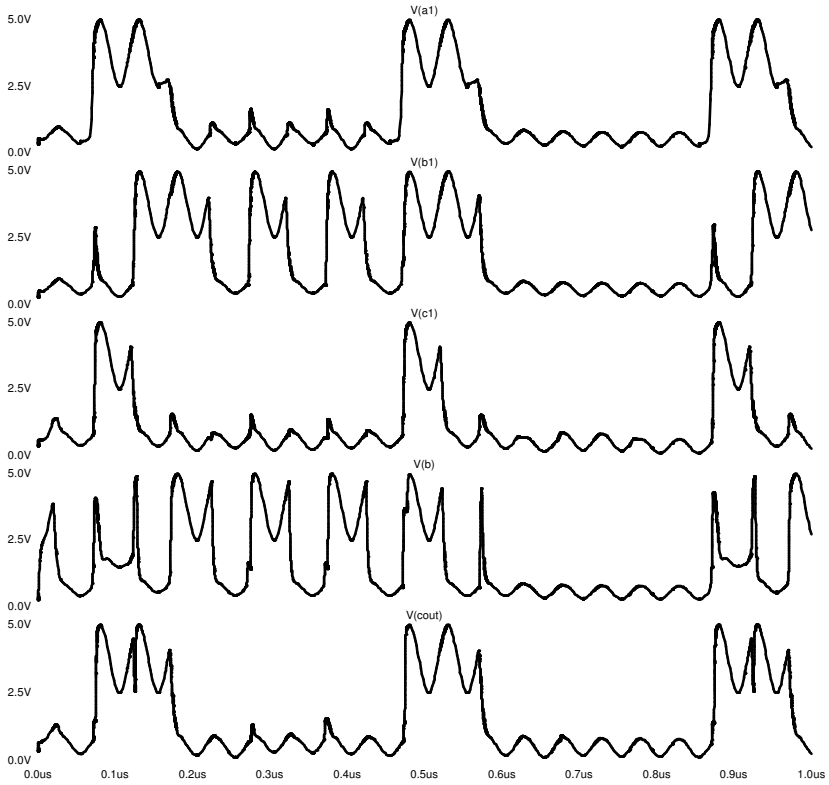

Fig. 6 4×4-bit 2PASCL multiplier at 10 MHz f_T using W=5.0μ at B full adder of p_3 .

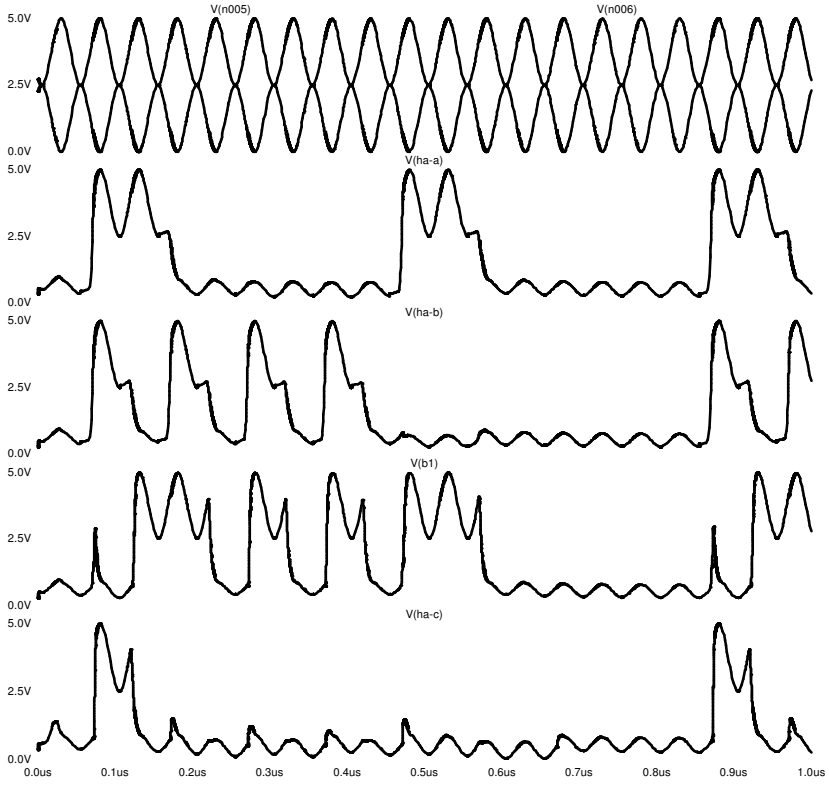

Fig. 7 4×4-bit 2PASCL multiplier at 10 MHz f_T using W=5.0μ at B1 half adder of p_3 .