4×4-bit 2PASCL Multiplier Simulation using 1.2μm process : evaluation on half adders.

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Abstract

The paper demonstrate the simulation results of the new half adders which was previously used in the simulation. The main objective is to remove the ripple and reduce the LO signal as low as possible. We also try to evaluate different type of full adder design for the same purpose. Finally the comparison of 4×4-bit 2PASCL multiplier using 1.2 μm process is carried out.

1 Introduction

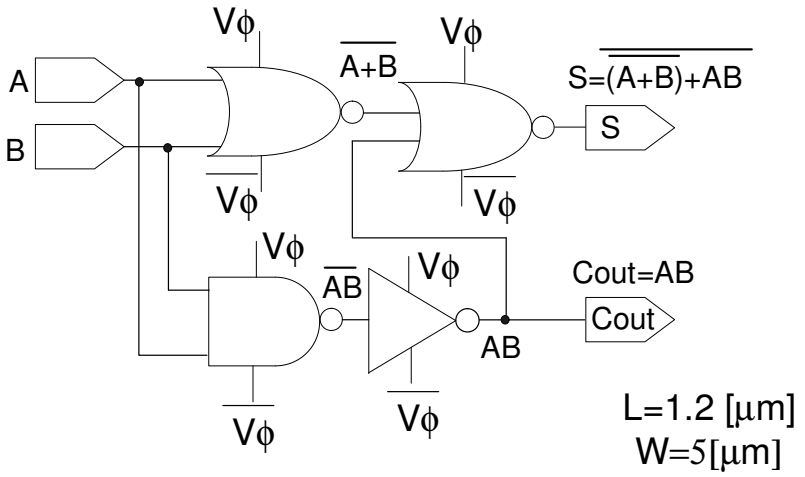
From previous study, we found that the effect of nMOS and pMOS diodes W and L is minimum to reduce the ripple and LO level. Thus, we evaluate another half adder and full adder to see if the is any improvement.W/L of the logic transistors used in the simulations are $5.0\mu/1.2$ μ.

2 Results

The results are shown in Fig. 1 to Fig. 19.

3 Conclusion

The SPICE simulation of 2PASCL logics using 1.2μ CMOS procees which leads to the fabrication has been carried to inspect the cause for the higher "0" signal level and ripples. From the results, we still haven't found the cause after evaluating some other half adders and full adders.



Block diagram of 2PASCL Half-adder

Fig. 1 The previous 2PASCL halfadder design.

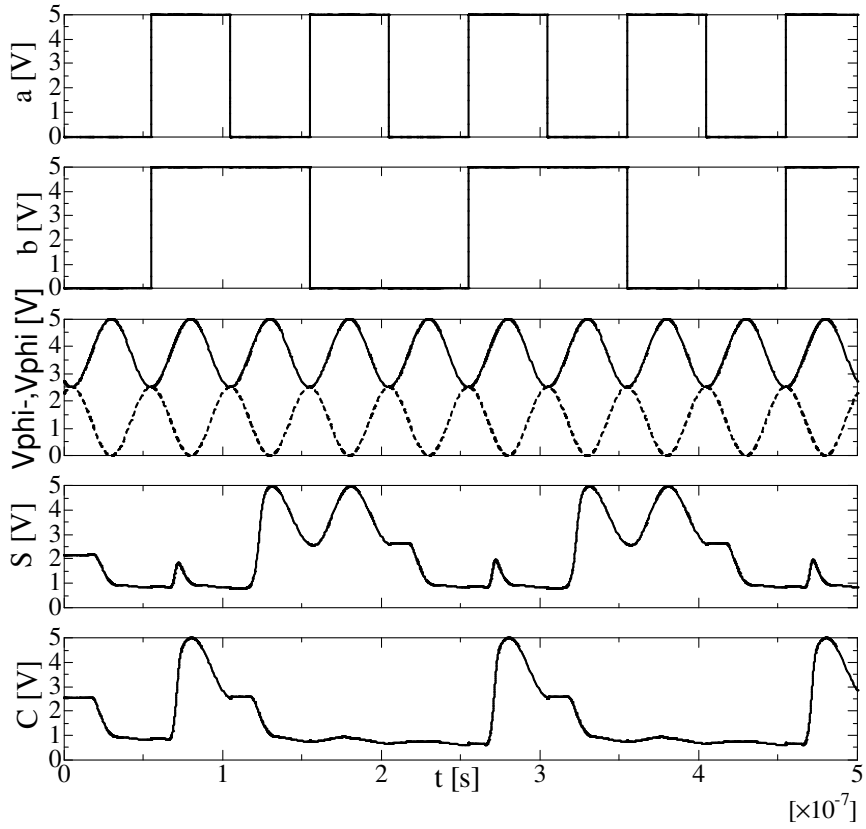


Fig. 2 Half adder using old block diagram at 10 MHz.

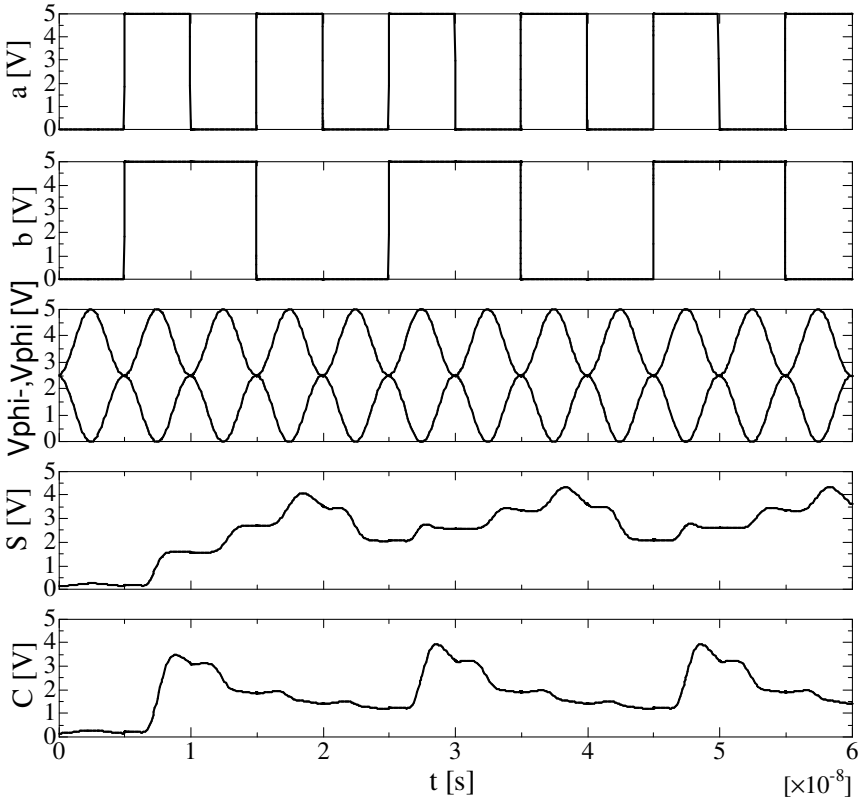


Fig. 3 Half adder using old block diagram at 50 MHz.

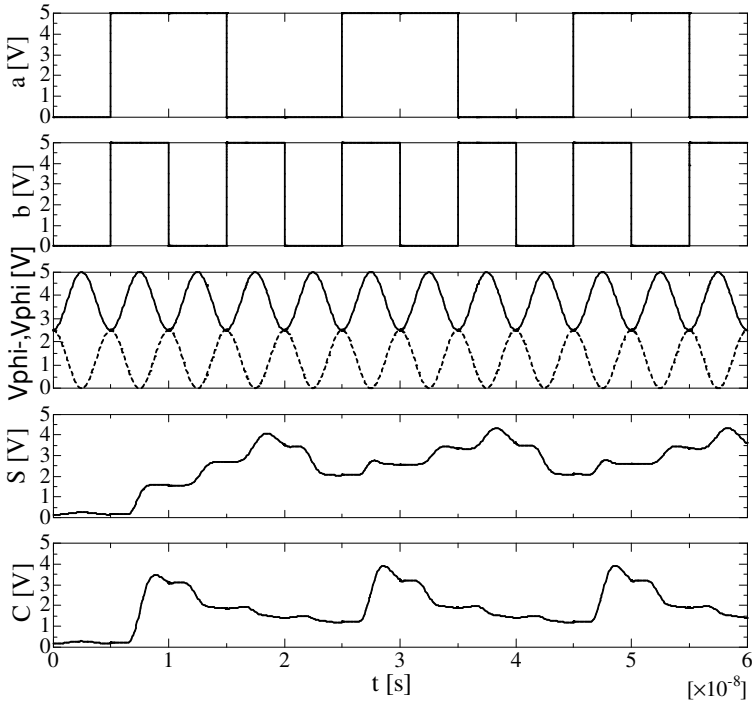


Fig. 4 Half adder using old block diagram at 100 MHz.

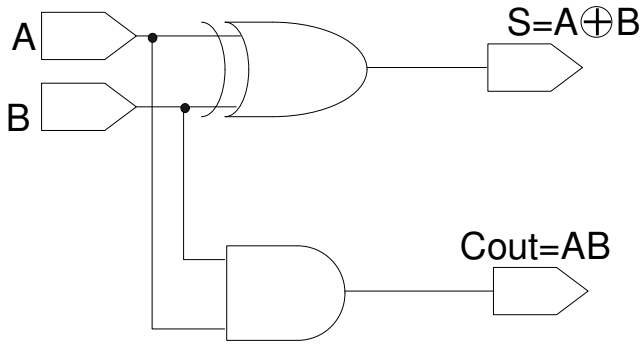


Fig. 5 The new half adder block diagram.

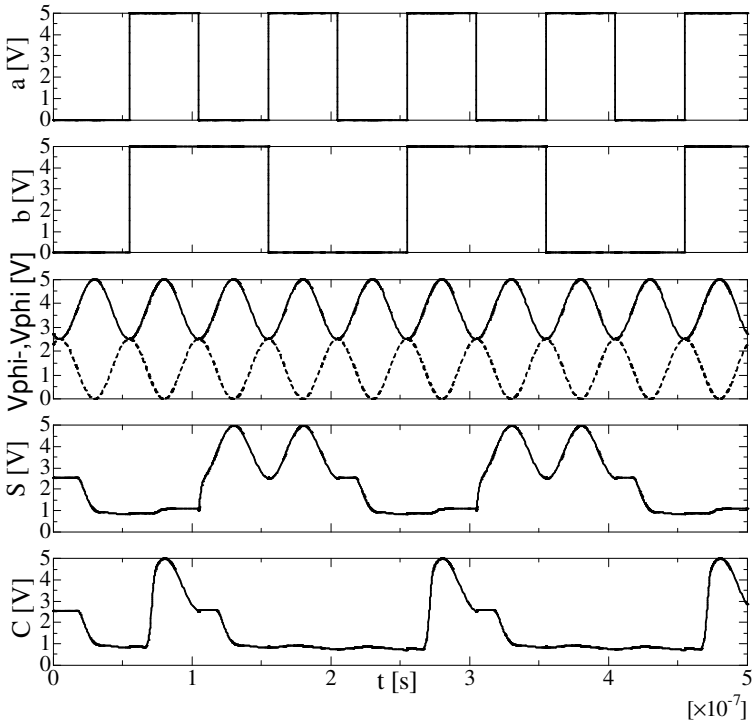


Fig. 6 Half adder using new block diagram at 10 MHz.

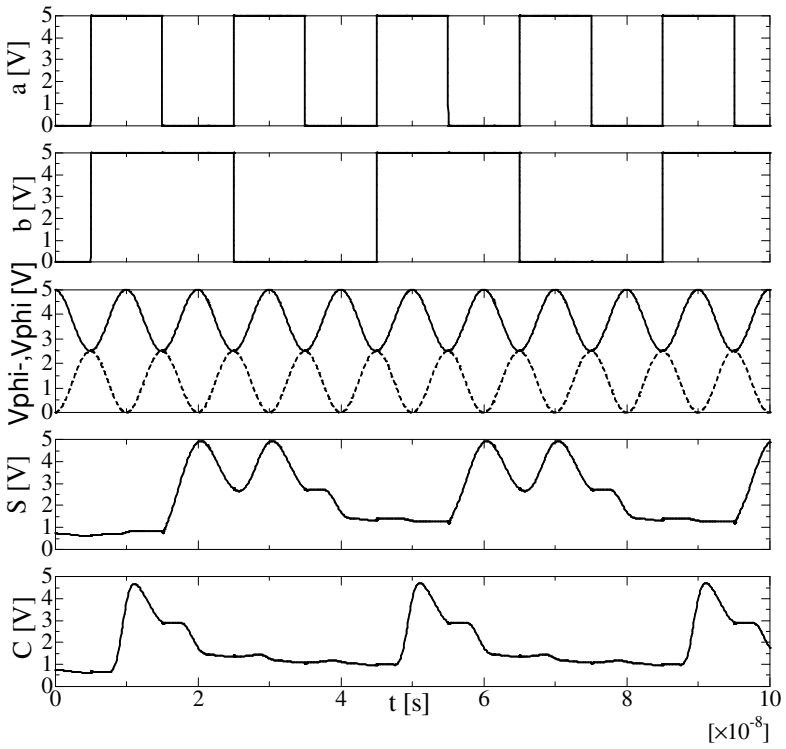


Fig. 7 Half adder using old block diagram at 50 MHz.

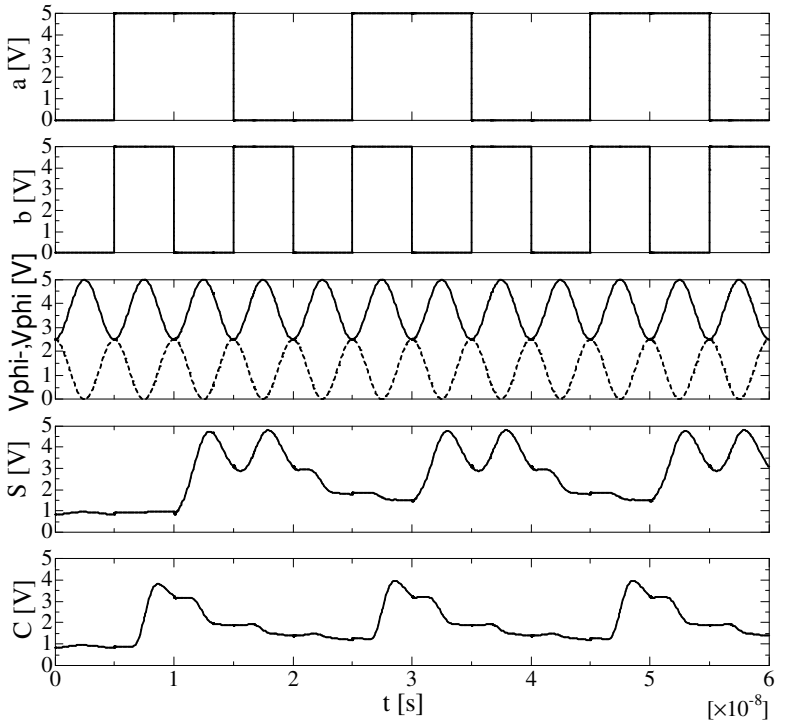


Fig. 8 Half adder using old block diagram at 100 MHz.

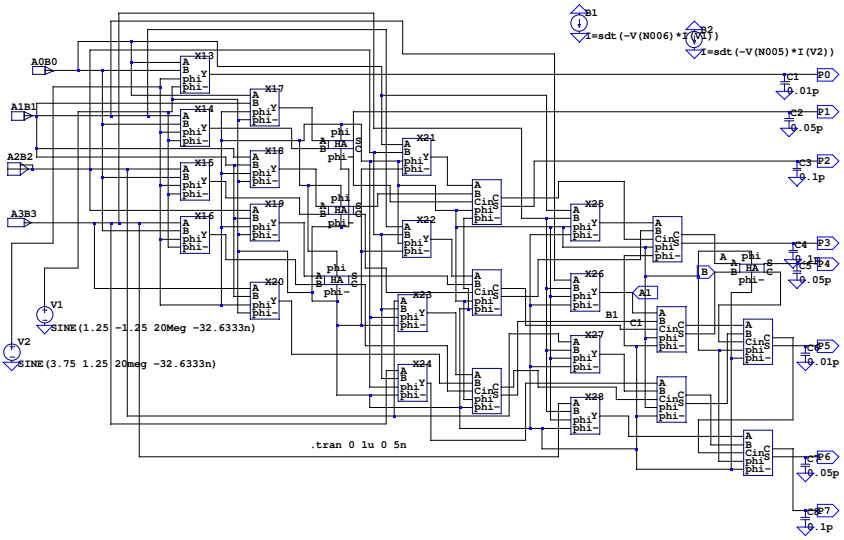


Fig. 9 Half adder using old block diagram at 100 MHz.

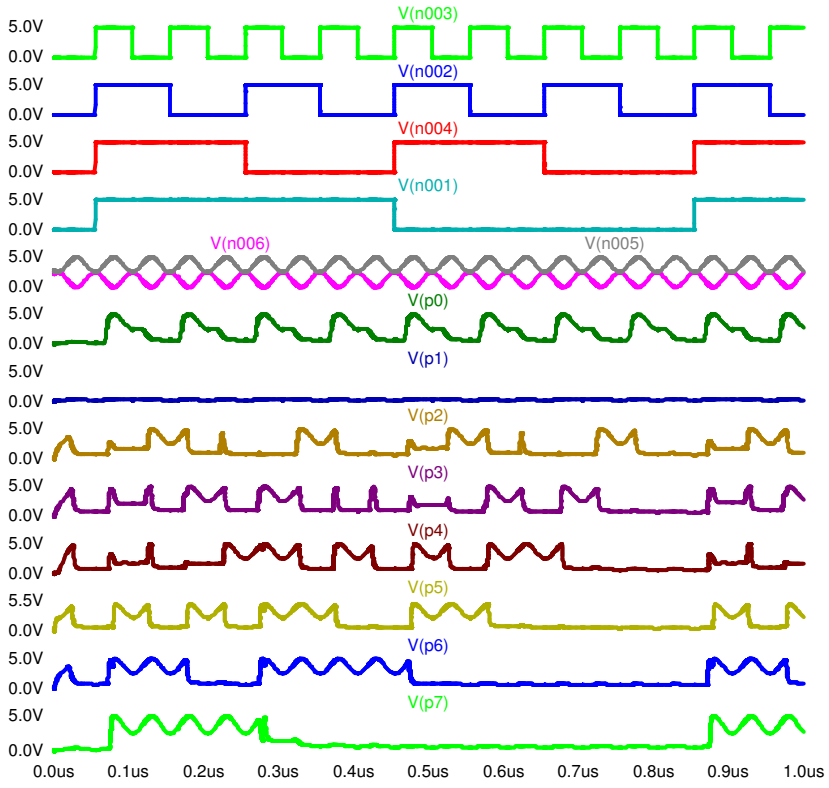


Fig. 10 Output of 2PASCL multiplier using new half adder block diagram at 10 MHz.

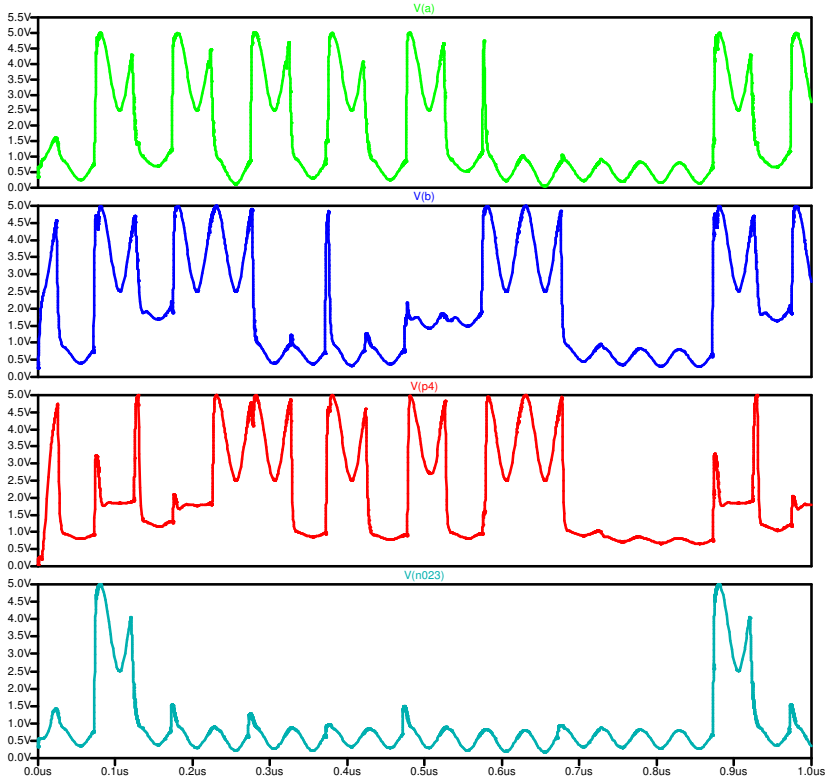


Fig. 11 Output of 2PASCL multiplier using new half adder block diagram at 10 MHz; focus at P4 output.

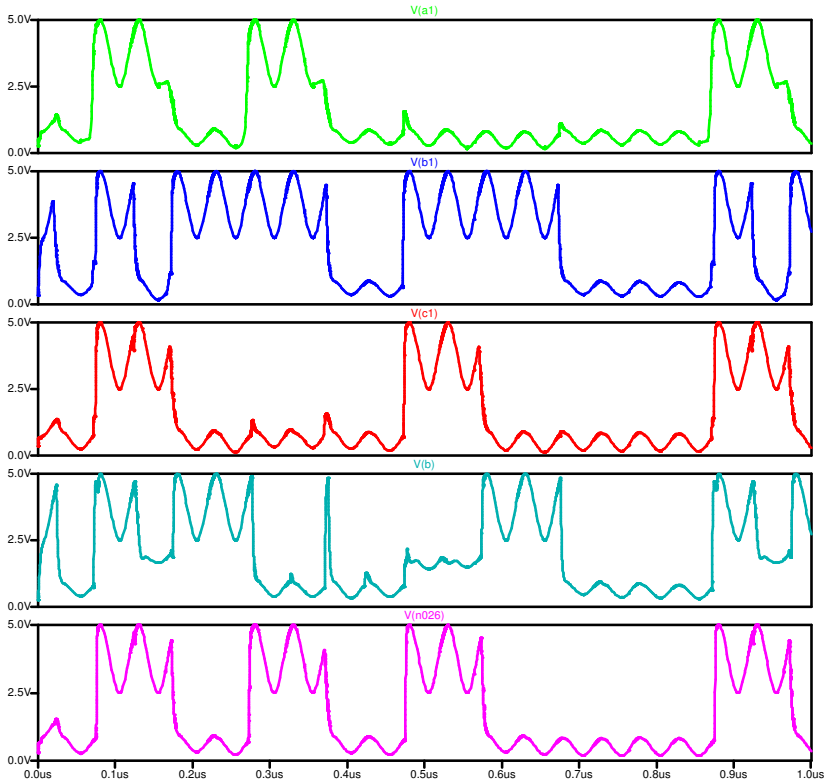
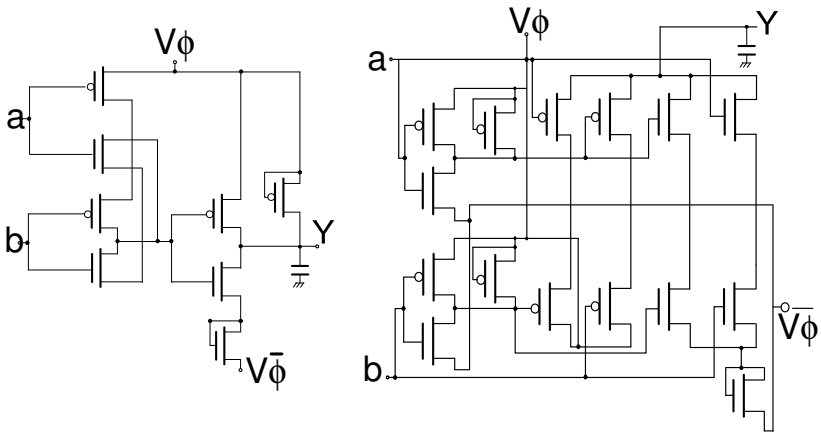


Fig. 12 Output of 2PASCL multiplier using new block diagram at 10 MHz; close-up at full adder beforeP4 output.



(a) (new) 2PASCL 2XOR (b) (old) 2PASCL 2XOR

Fig. 13 Old and new diagram of 2PASCL XOR.

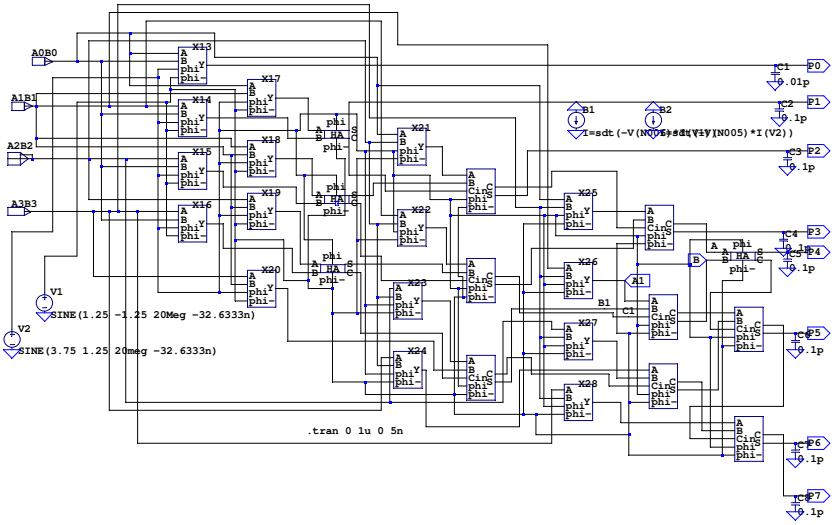


Fig. 14 Old and new diagram of 2PASCL XOR.

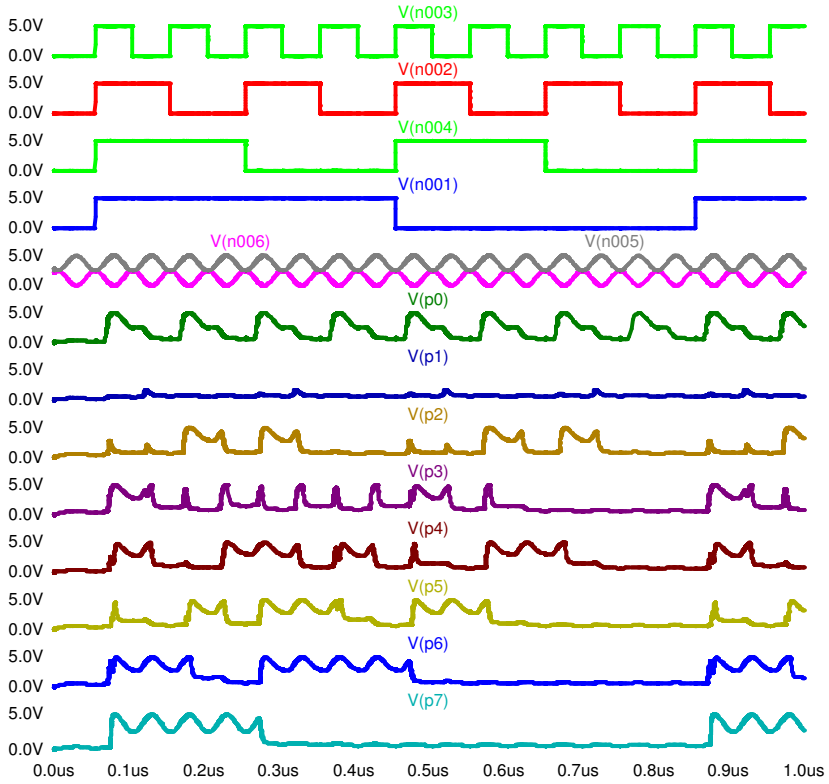


Fig. 15 Output of 2PASCL multiplier using old XOR design.

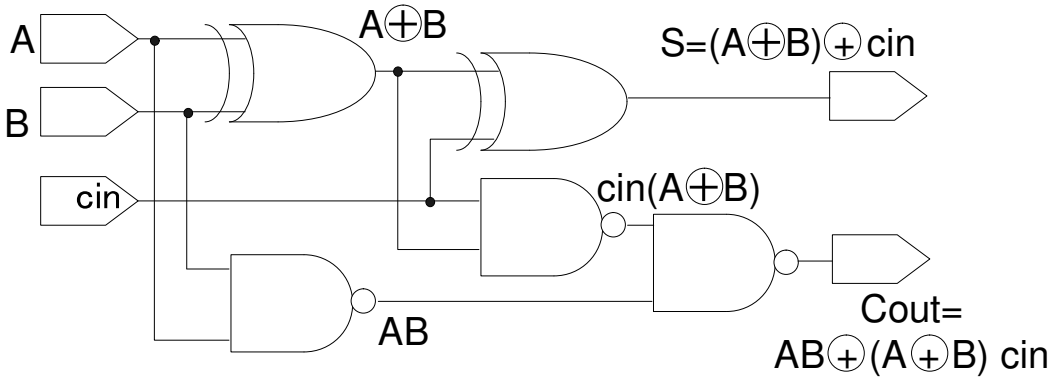


Fig. 16 Existing full adder diagram.

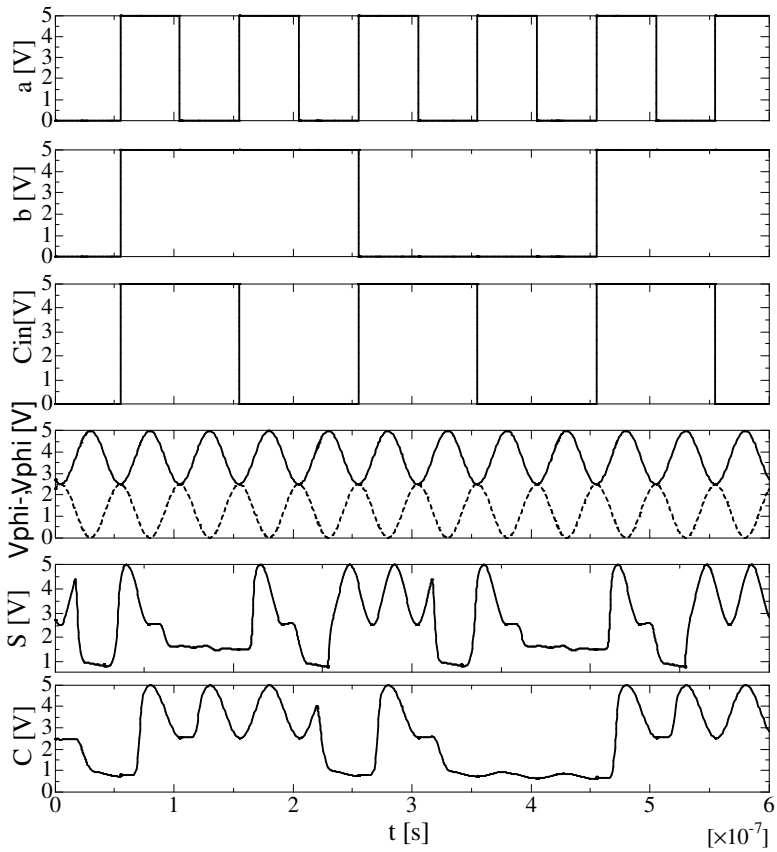


Fig. 17 Output of existing 2PASCL full adder at 10 MHz.

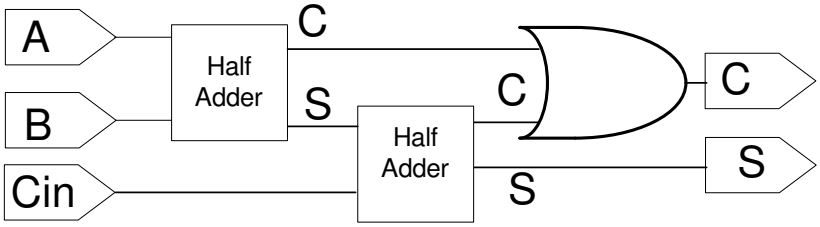


Fig. 18 New design of full adder.

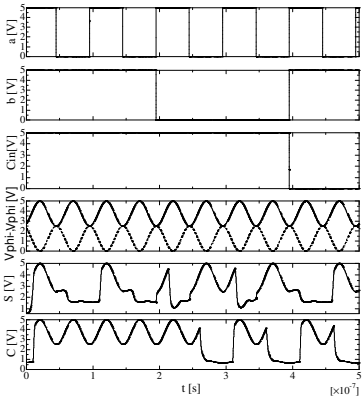


Fig. 19 Output of new full adder design at 10 MHz.