Electrical current evaluation of 2PASCL and CMOS

Nazrul Anuar

Graduate School of Engineering, Gifu University, Gifu, 501-1193 Japan

Abstract

The paper demonstrate the simulation results current condition during transition. The main objective is to find the MOS where the highest power is dissipated.

1 Introduction

Significant low power dissipation for 2PASCL compared to CMOS. Sudden current flow during transition resulting in a large current flowing though the resistive element in pMOS during charging. In this study, we compare the drain current and source current flowed during transition in 2PASCL NOT circuit and conventional CMOS.

2 2PASCL vs. CMOS

The circuit diagram and the current conditions are as shown in the Fig. 1 and Fig. 2

3 Results

The results are shown in Fig. 3 to Fig. 6.

4 Conclusion

From the simulation result, 2PASCL reduces 27.2 % of maximum current flow through M2 as compared to CMOS.

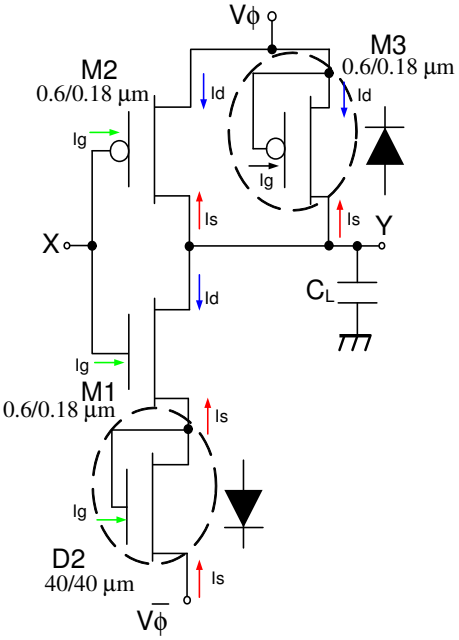

Fig. 1 2PASCL NOT circuit with flowing current symbols.

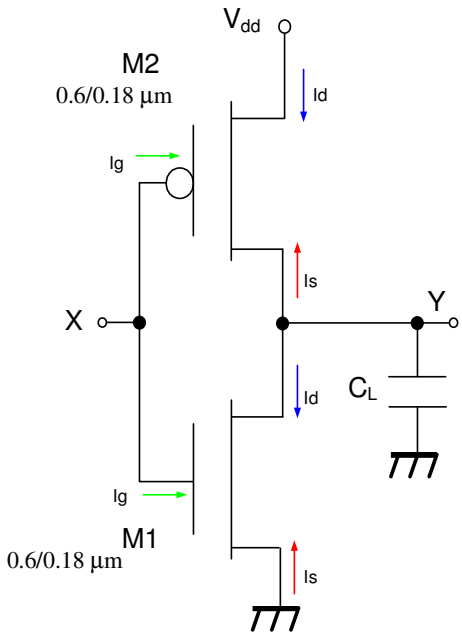

Fig. 2 CMOS NOT circuit with flowing current symbols.

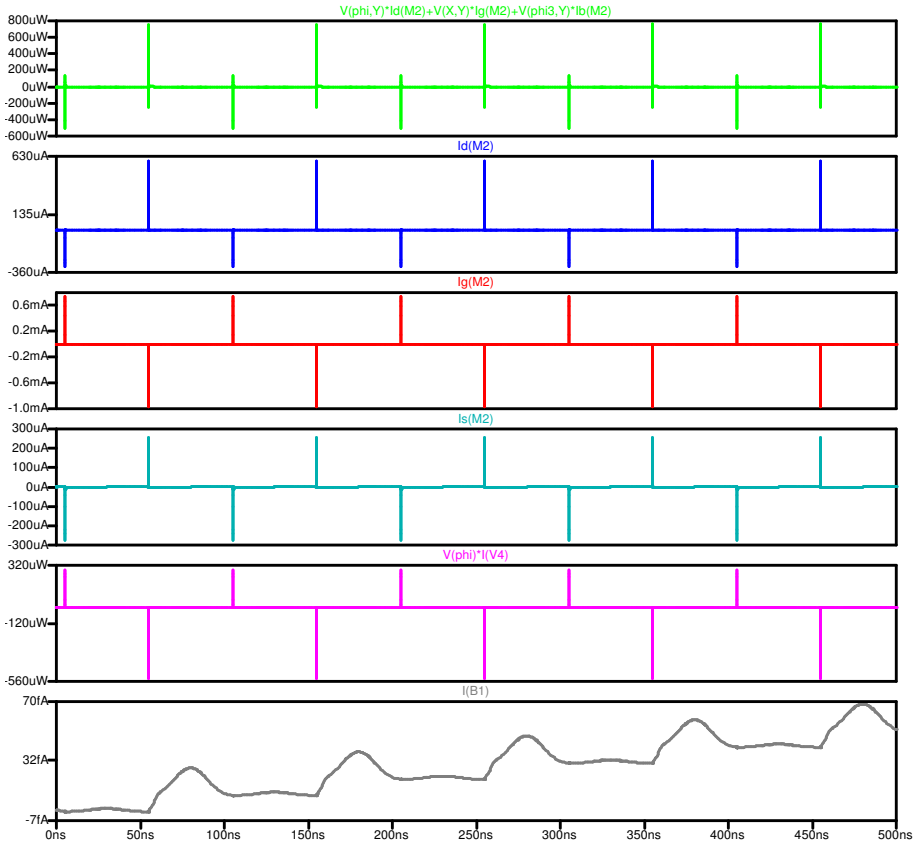

Fig. 3 2PASCL NOT current condition at M2 pMOS.

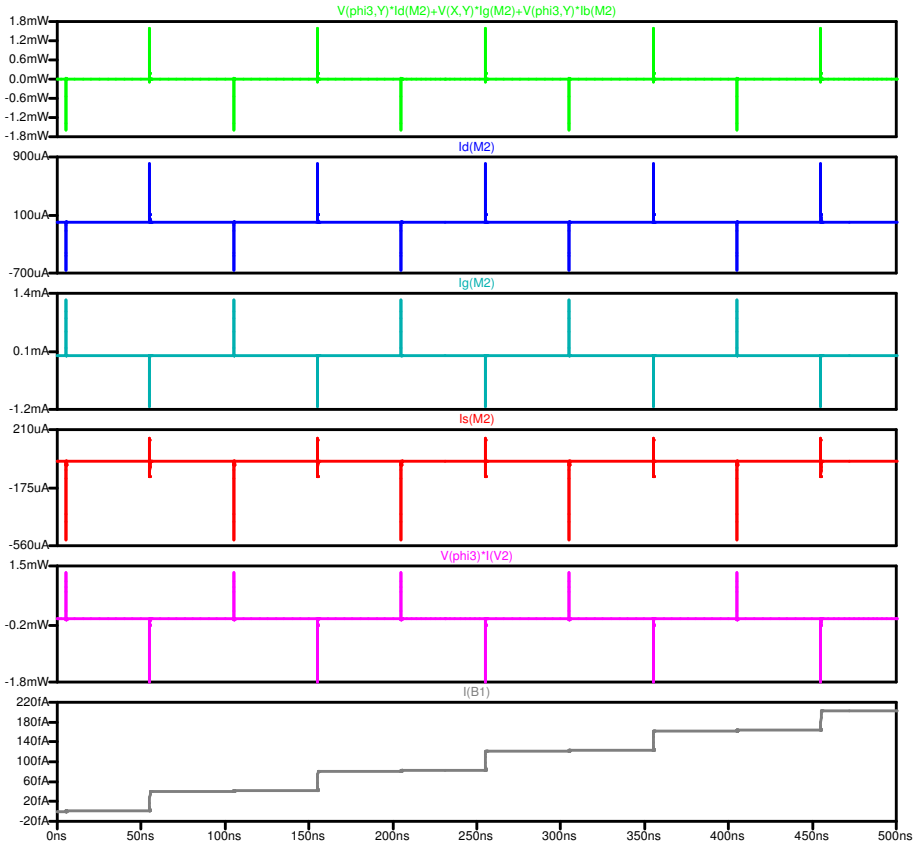

Fig. 4 CMOS current condition at M2 pMOS.

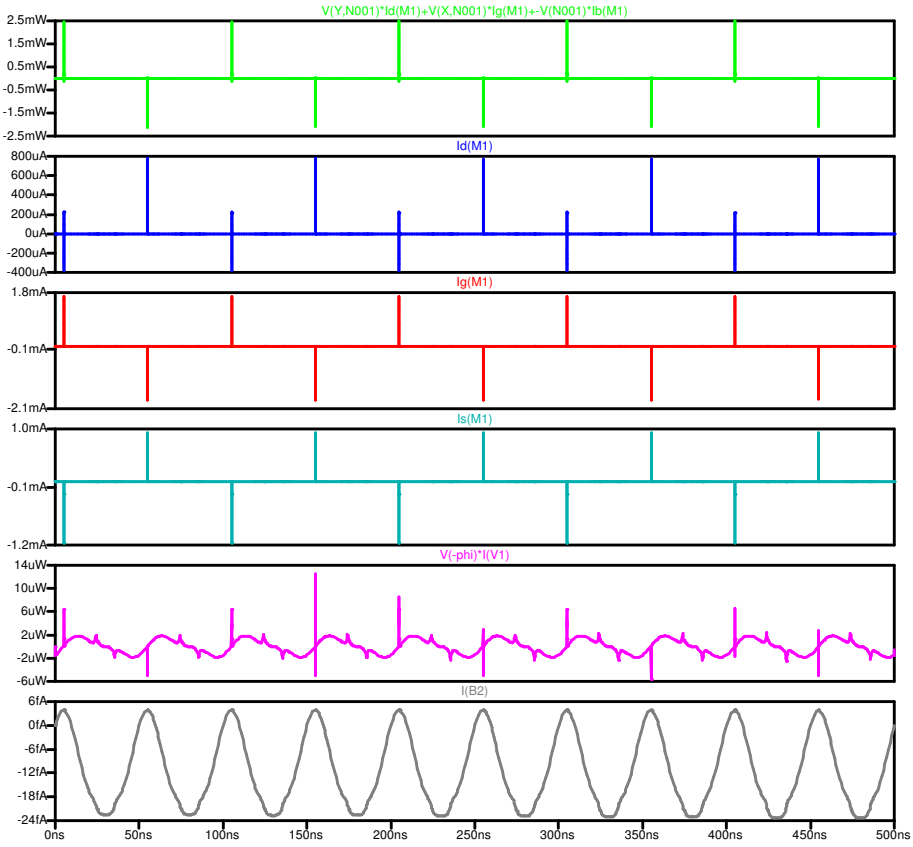

Fig. 5 2PASCL NOT current condition at M1 nMOS.

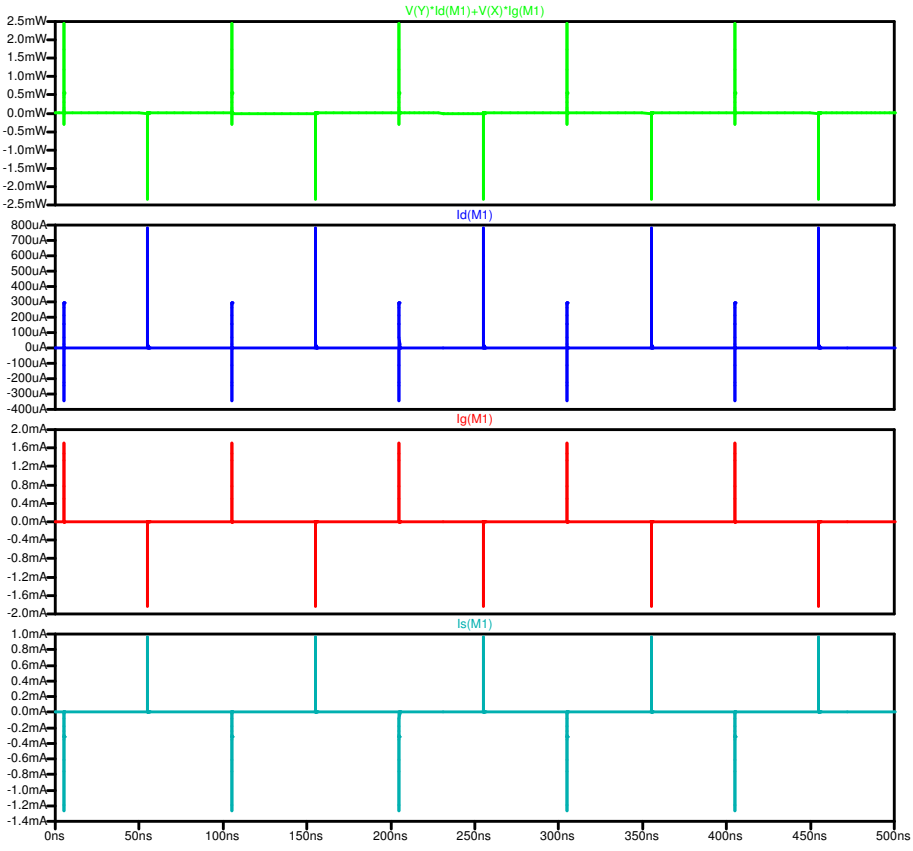

Fig. 6 CMOS current condition at M1 nMOS.

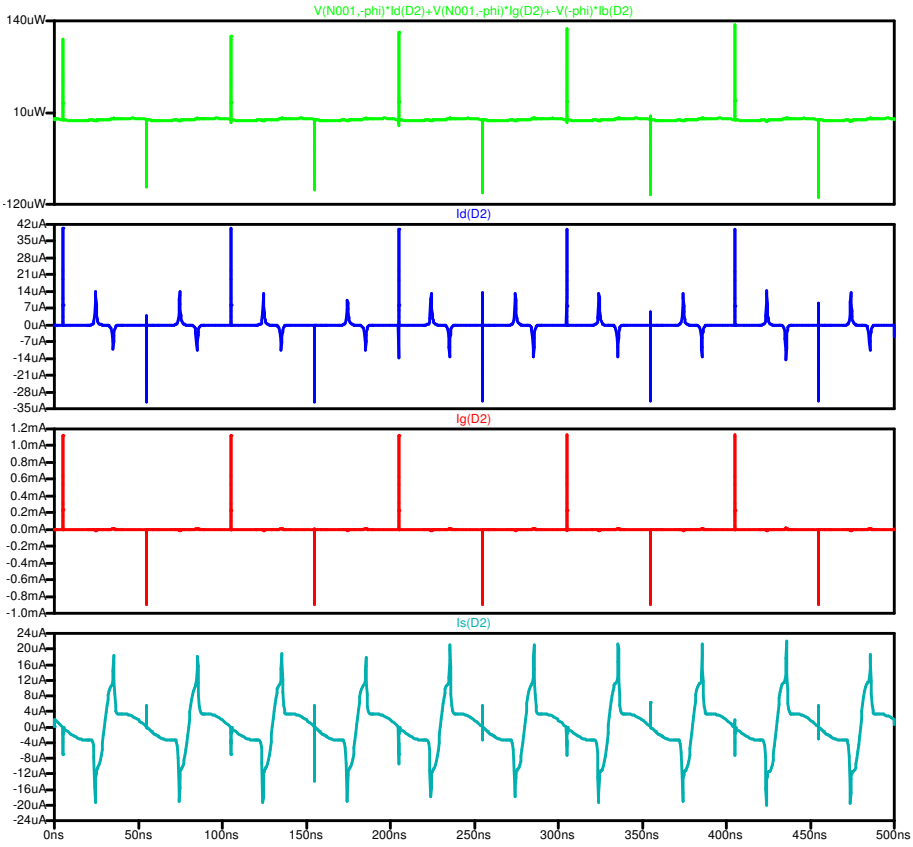

Fig. 7 2PASCL NOT current condition at D2 nMOS diode.

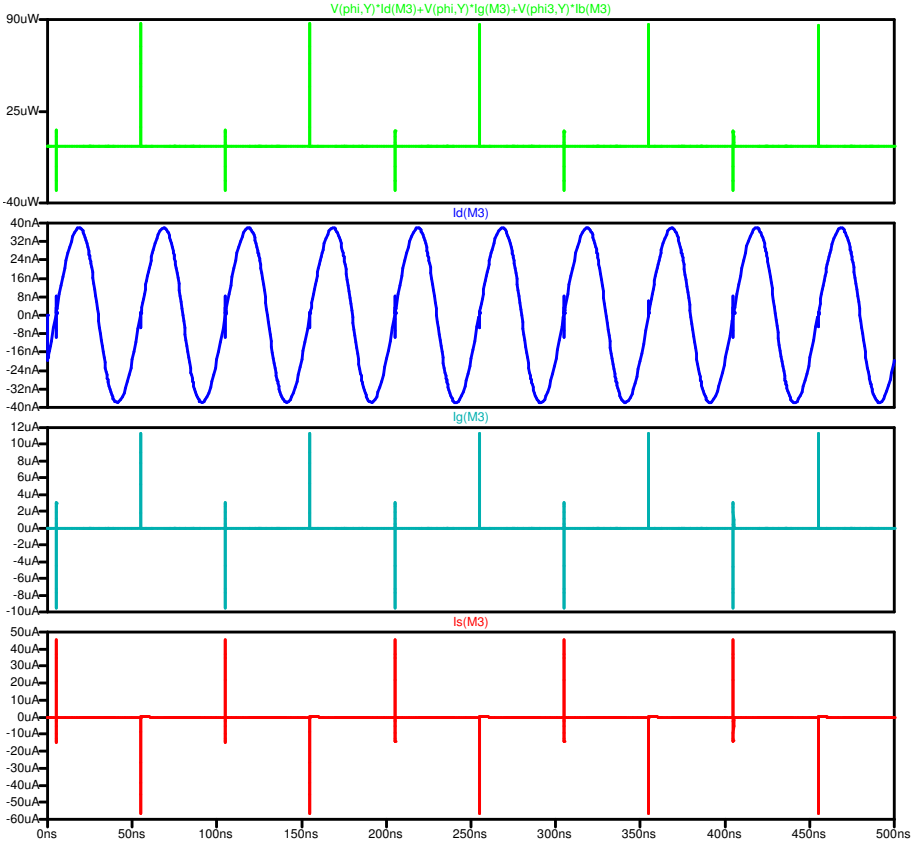

Fig. 8 2PASCL NOT current condition at M3 pMOS diode.