# Evaluation on electrical current and energy dissipation at every transistor of 2PASCL/CMOS and MOSFET diode characteristic study

Nazrul Anuar

Graduate School of Engineering, Gifu University, Gifu, 501-1193 Japan

**Abstract**

The paper demonstrate the simulation results of 2PASCL and CMOS. The objective is to find what is the amount of current flow and the highest dissipated energy of MOS transistor.

## 1 Introduction

In this paper we compare the current flow through the MOS transistors in 2PASCL and CMOS. We also compare the energy dissipation at every MOS transistor.

## 2 2PASCL vs. CMOS

The circuit diagram and the current conditions are as shown in the Fig. 1 and Fig. 2, respectively

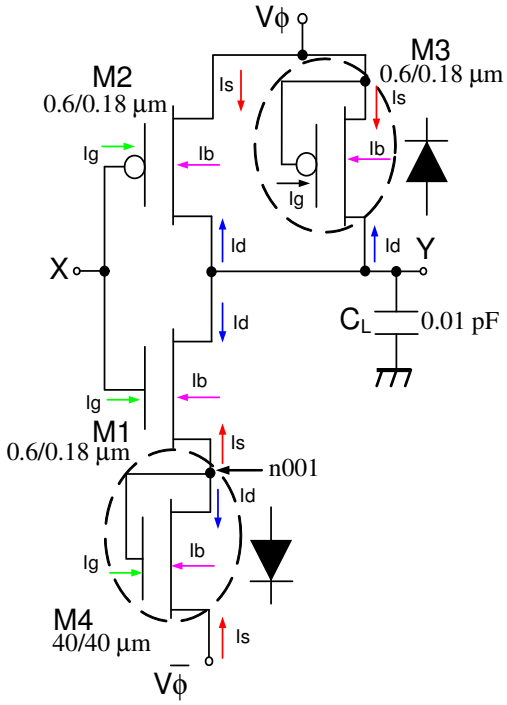


Fig. 1 2PASCL NOT circuit with flowing current symbols.

## 3 Results

### 3.1 Current flow evaluation

The results of this evaluation are as follows: 2PASCL at 10 MHz input clock in Fig. 3 and conventional CMOS at 10 MHz input clock is shown in Fig. 4.

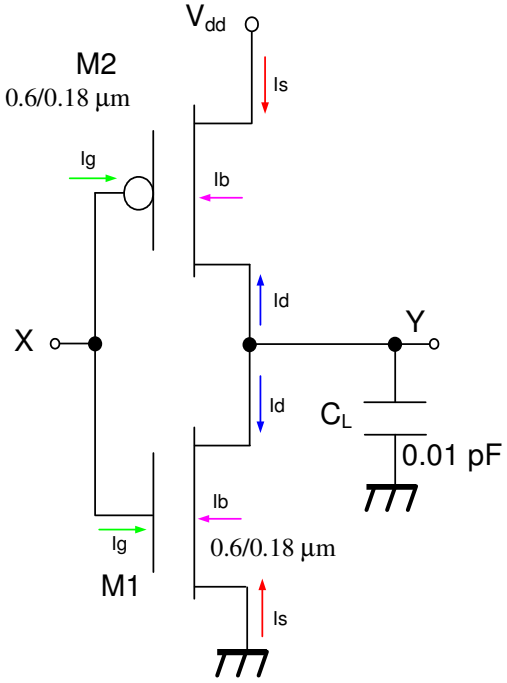


Fig. 2 CMOS NOT circuit with flowing current symbols.

#### 3.1.1 Details of calculation

**2PASCL NOT**

- I(B1)=sdt((V(y)-V(n001))*(-Is(M1))) — dissipated energy at M1
- I(B2)=sdt((V(phi)-V(y))*(-Id(M2))) — dissipated energy at M2
- I(B3)=sdt((V(y)-V(phi))*Id(M3)) — dissipated energy at M3
- I(B4)=sdt((V(n001)-V(-phi))*Id(M4)) — dissipated energy at M4
- I(B5)=sdt(-V(phi)*I(V4))— supplied energy calculated at the power supply (phi)
- I(B6)=sdt(-V(-phi)*I(V1))— supplied energy calculated at the power supply (-phi)

**CMOS NOT**

- I(B1)=sdt(V(y)*(-Is(M1)) — dissipated energy at M1
- I(B2)=sdt((V(Vdd)-V(y))*(-Id(M2)) — dissipated energy at M2

- I(B3)=sdt(V(Vdd)*I(V4)) — supplied energy calculated at the power supply (Vdd).
- I(BF1)=sdt(V(y2)*(-Is(M12)) — dissipated energy at M1 (using trapezoidal power clock)
- I(BF2)=sdt((V(Vdd2)-V(y2))*(-Id(M22)) — dissipated energy at M2 (using trapezoidal power clock)
- I(BF3)=sdt(V(Vdd2)*I(V6)) — supplied energy calculated at the power supply (Vdd) (using trapezoidal power clock).

#### 3.1.2 Diodes in 2PASCL characteristic

The results are as shown in Figs.5–10

## 4 Conclusion

From the simulation result, adiabatic switching during charging reduces the energy dissipation significantly by reducing the current flow.

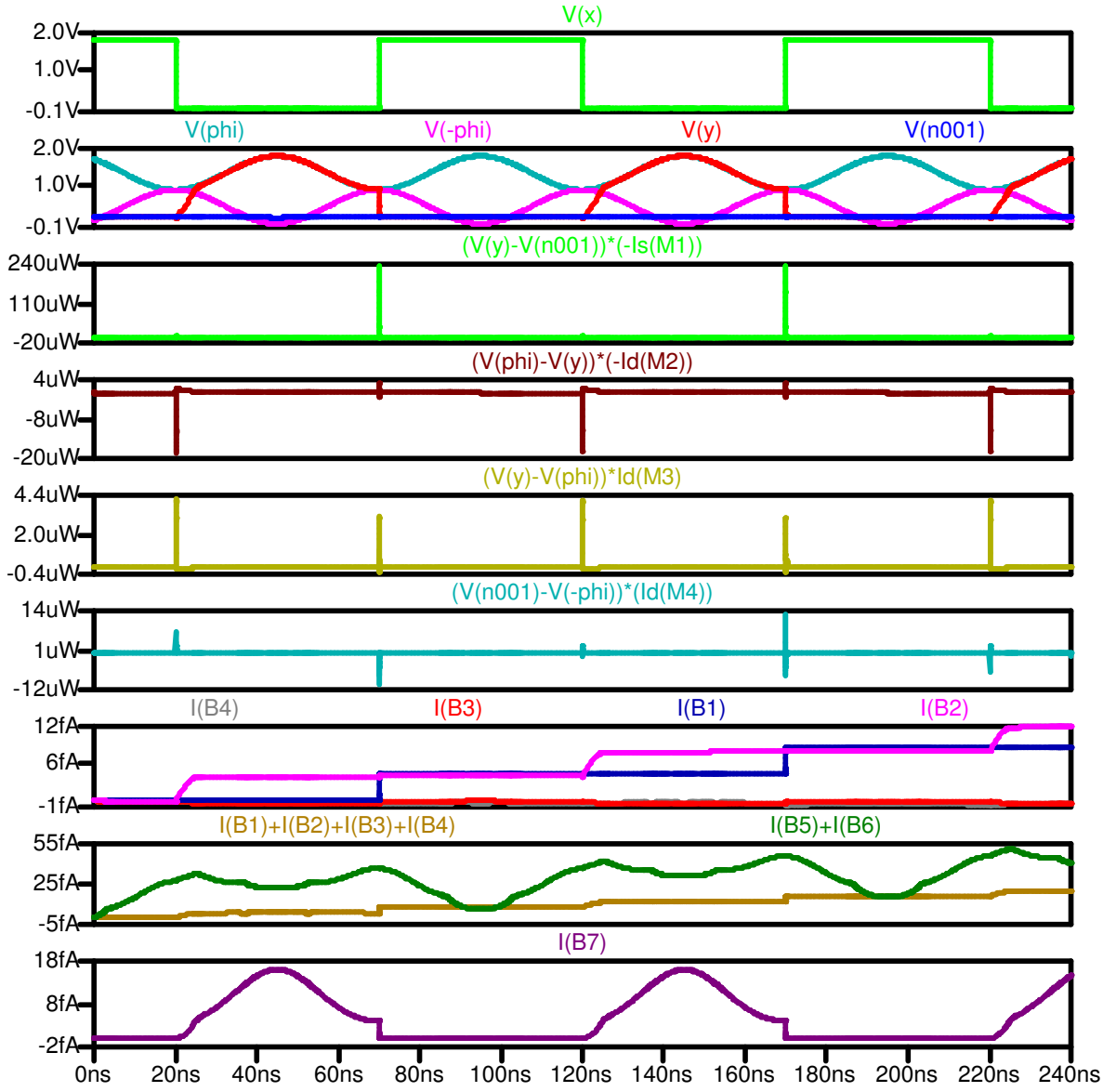


Fig. 3 2PASCL NOT voltage, current and dissipation energy characteristic at 10 MHz input frequency.

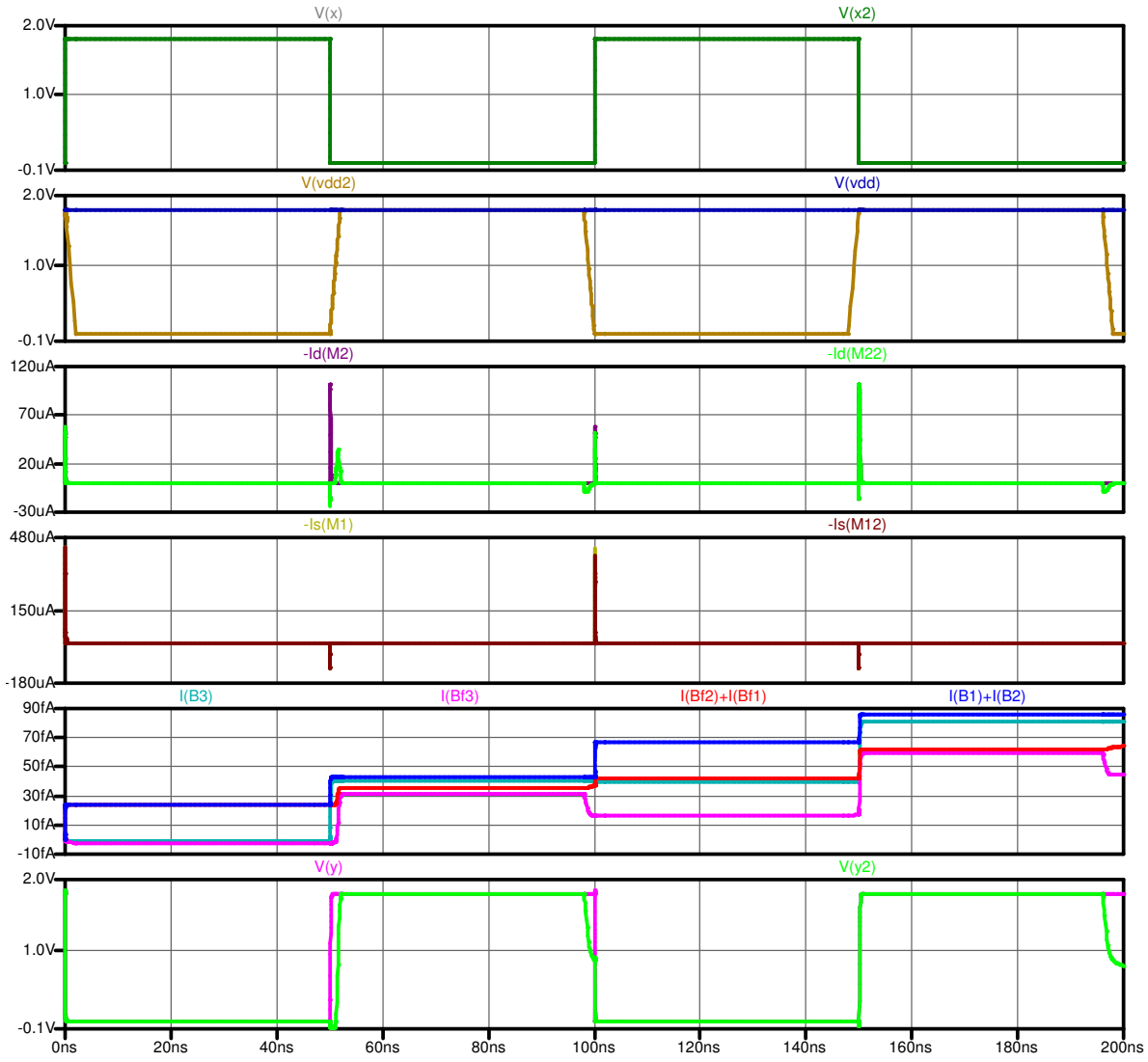


Fig. 4 CMOS NOT voltage, current and dissipation energy characteristic comparison using Vdd=1.8 V and trapezoidal power clock with the height of 1.8 V.

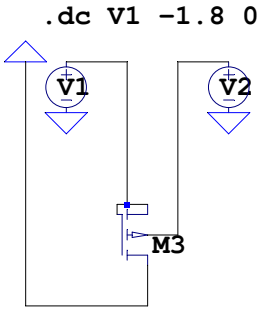


Fig. 5 pMOS SPICE diagram

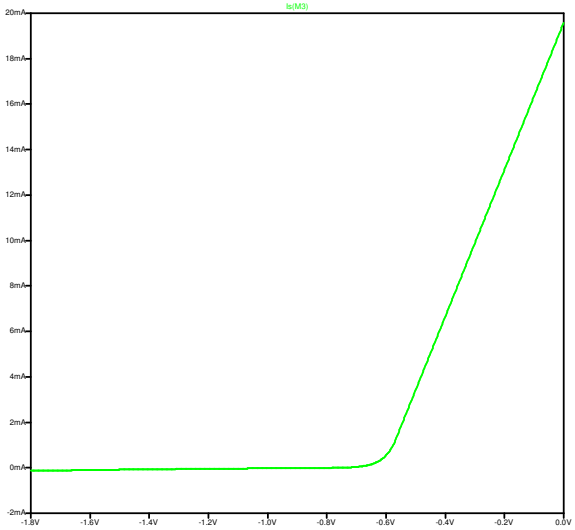


Fig. 6 Id-Vds

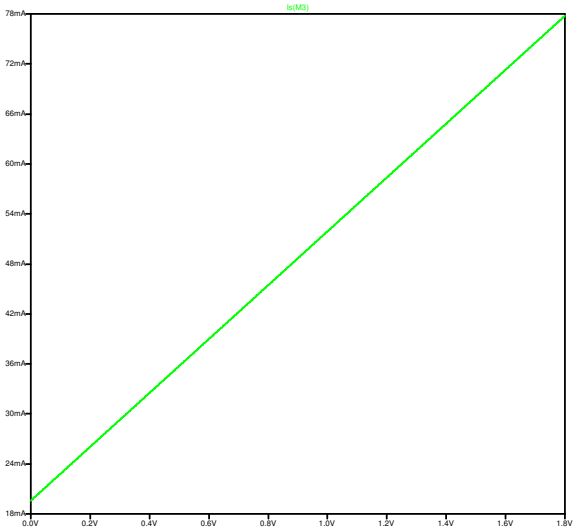


Fig. 7 Id-Vds

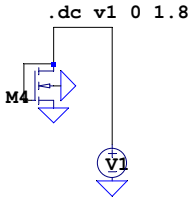


Fig. 8　nMOS SPICE diagram

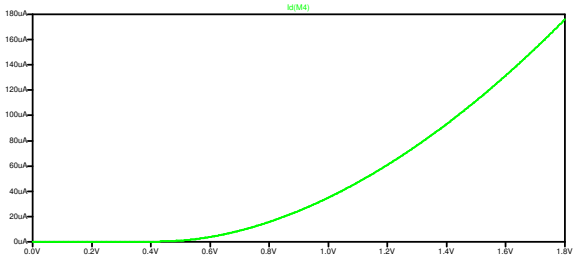


Fig. 9　Id-Vds

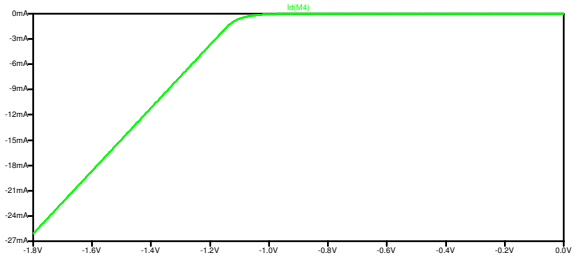


Fig. 10　Id-Vds