Current characteristic study

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Abstract

1 Objective

2 Analysis

2.1 Diode characteristic of 2PASCL inverter

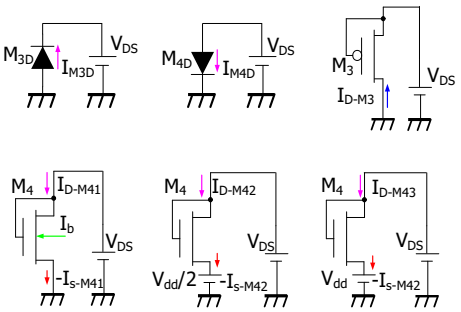

Fig. 1 Evaluation on the generic and MOSFETs diodes used in 2PASCL.

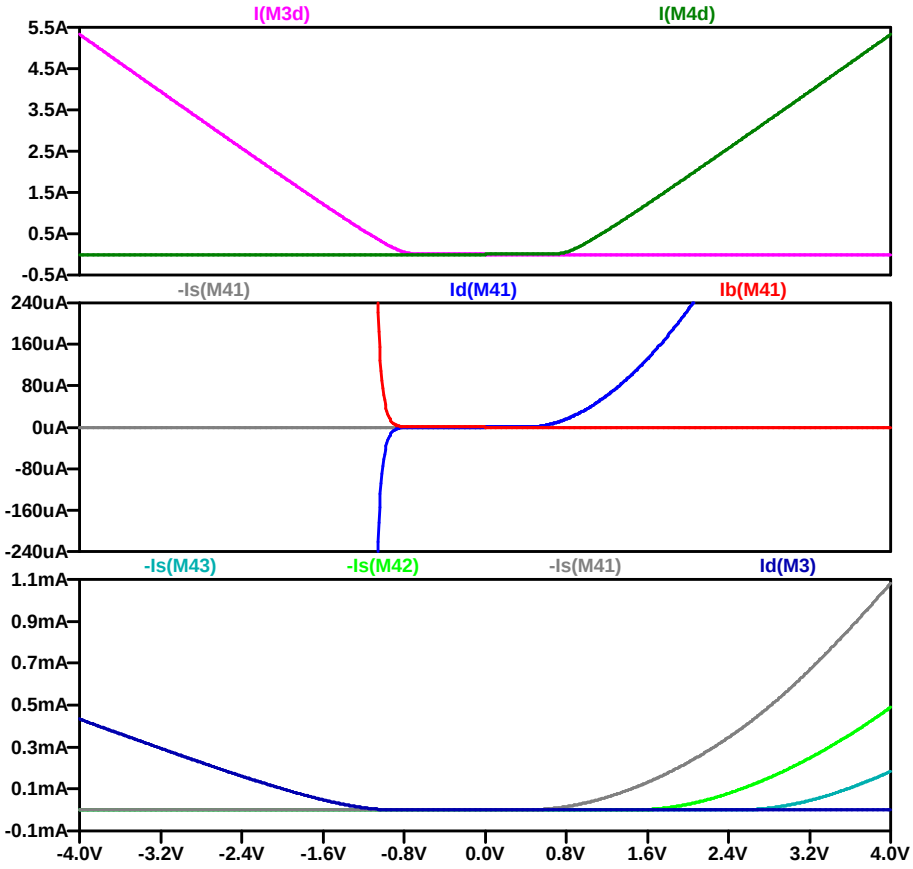

Fig. 2 Current flow in the transistors vs. drain-source voltage (V_{DS}).

2.2 Analysis of 2PASCL inverter operation

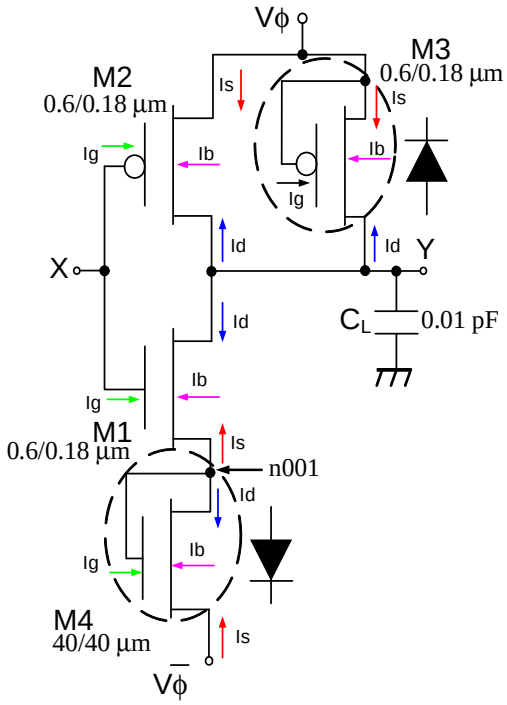

Fig. 3 2PASCL NOT circuit with flowing current symbols.

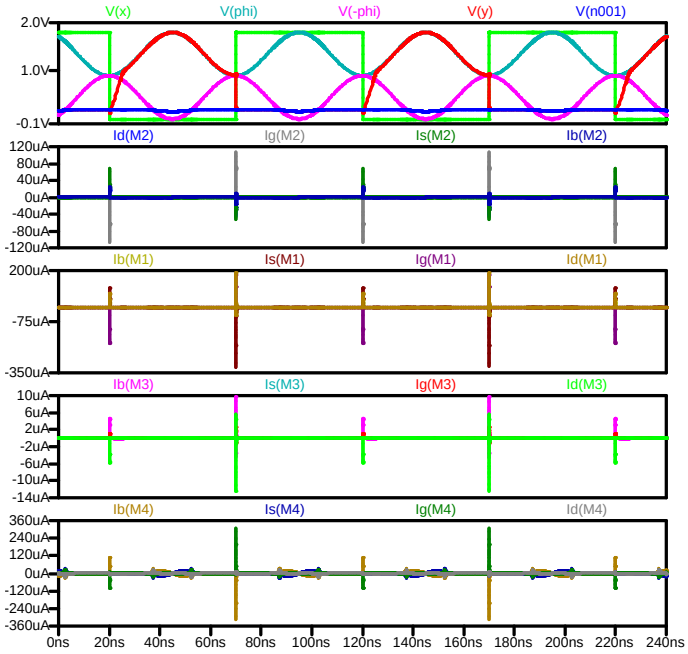

Fig. 4 2PASCL NOT voltage, current at each transistors for input frequency is 10 MHz.

2.2.1 Details of calculation

2PASCL NOT

- I(B1)=sdt((V(y)-V(n001))*(-Is(M1))) — dissipated energy at M1
- I(B2)=sdt((V(phi)-V(y))*(-Id(M2))) — dissipated energy at M2
- I(B3)=sdt((V(y)-V(phi))*Id(M3)) — dissipated energy at M3
- I(B4)=sdt((V(n001)-V(-phi))*Id(M4)) — dissipated energy at M4
- I(B5)=sdt(-V(phi)*I(V4))— supplied energy calculated at the power supply (phi)
- I(B6)=sdt(-V(-phi)*I(V1))— supplied energy calculated at the power supply (-phi)

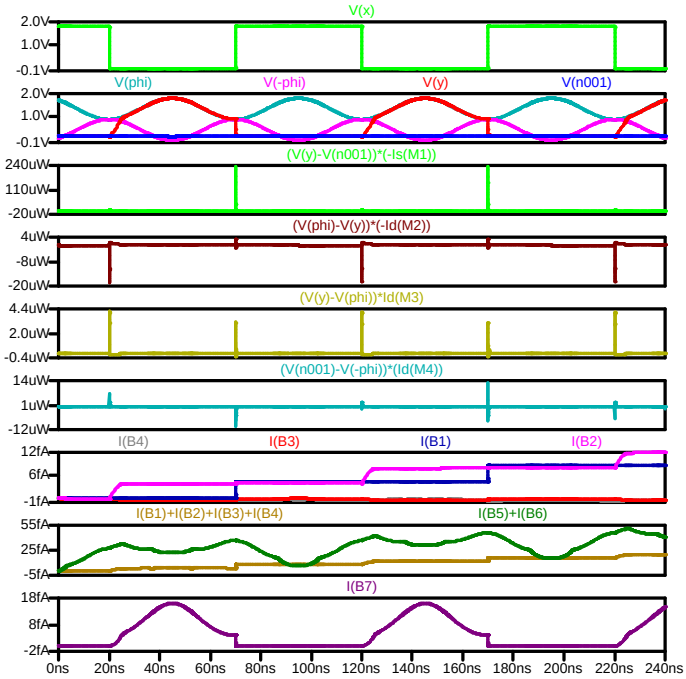

Fig. 5 2PASCL NOT current condition.

2.3 Analysis of 2PASCL inverter power dissipation

2.4 Analysis of 2PASCL inverter delay

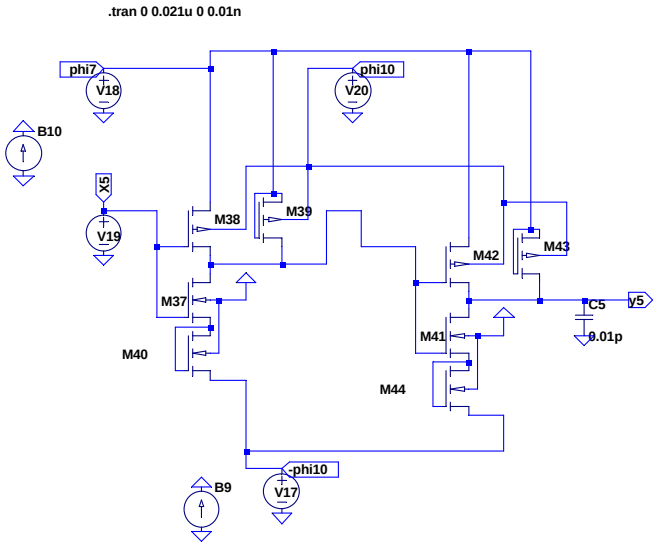

Fig. 6 2-inverter chain evaluation circuit diagram.

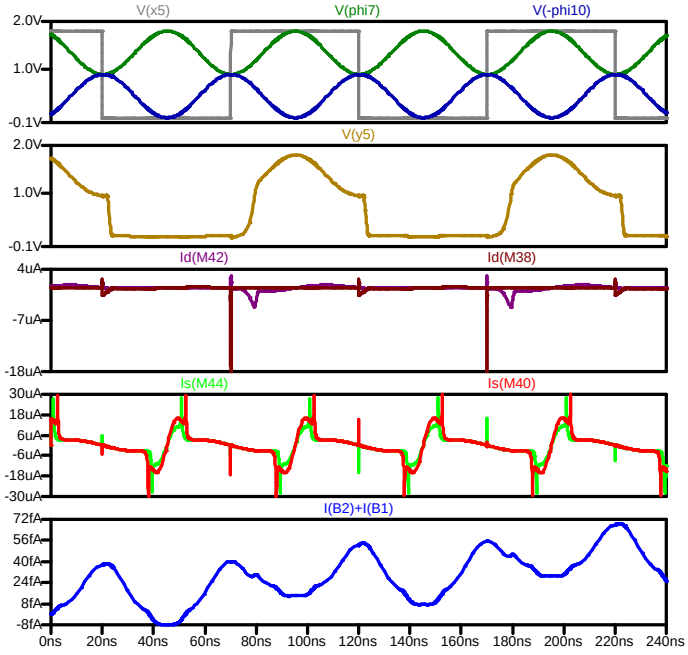

Fig. 7 2-inverter chain evaluation results from the simulation.

2.5 Analysis of 2PASCL inverter equivalent circuit

2.6 Analysis of 2PASCL inverter pass-through current

2.7 Analysis of Adiabatic CMOS inverter operation and power dissipation

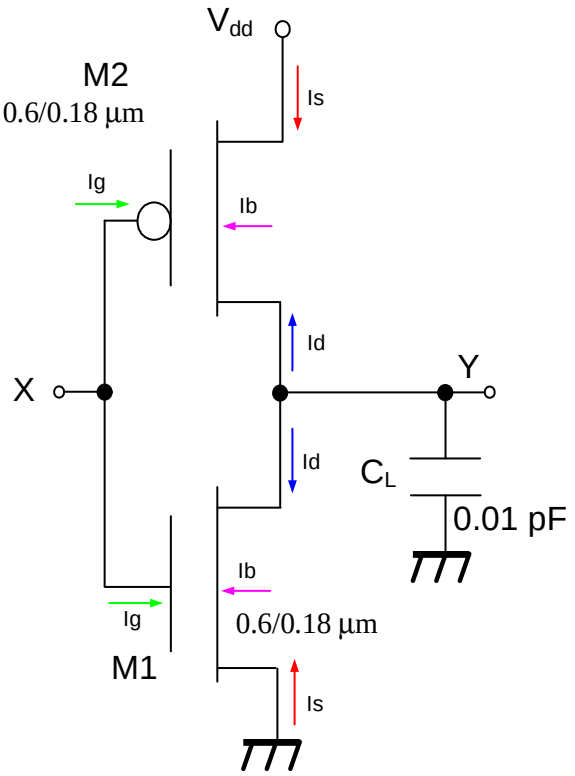

Fig. 8 CMOS NOT circuit with flowing current symbols.

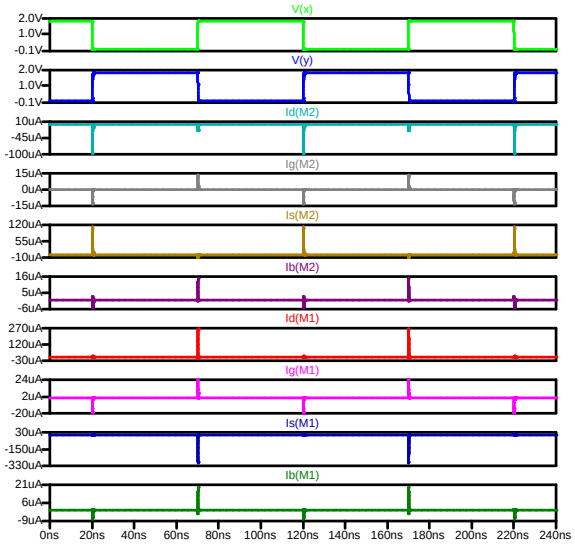

Fig. 9 CMOS current condition.

2.7.1 CMOS NOT

- I(B1)=sdt(V(y)*(-Is(M1)) — dissipated energy at M1
- I(B2)=sdt((V(Vdd)-V(y))*(-Id(M2)) — dissipated energy at M2
- I(B3)=sdt(V(Vdd)*I(V4)) — supplied energy calculated at the power supply (Vdd).

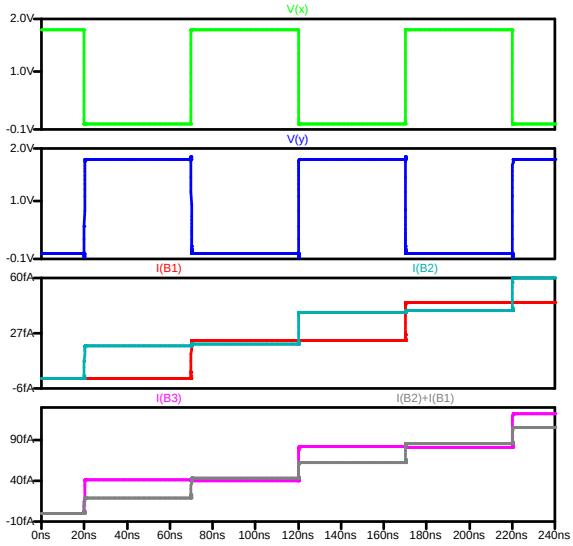

Fig. 10 CMOS NOT logic: energy dissipation at each transistor.

- I(BF1)=sdt(V(y2)*(-Is(M12)) — dissipated energy at M1 (using trapezoidal power clock)
- I(BF2)=sdt((V(Vdd2)-V(y2))*(-Id(M22)) — dissipated energy at M2 (using trapezoidal power clock)
- I(BF3)=sdt(V(Vdd2)*I(V6)) — supplied energy calculated at the power supply (Vdd) (using trapezoidal power clock).

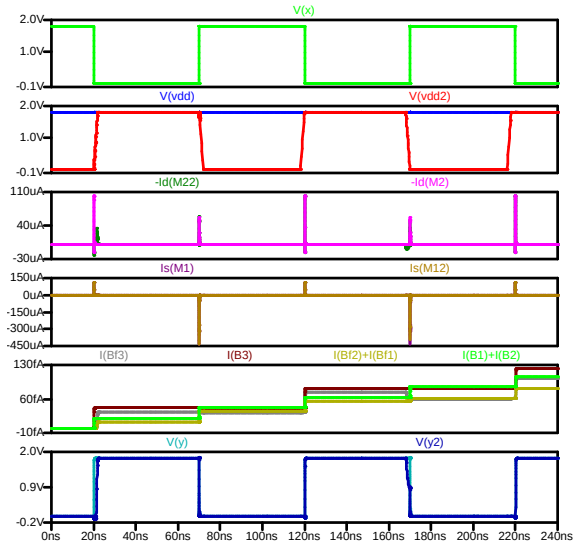

Fig. 11 CMOS NOT voltage, current and dissipation energy characteristic comparison using Vdd=1.8 V and trapezoidal power clock with the height of 1.8 V.

2.8 RC circuit opreation