RC circuit operation and power dissipation analysis

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1 Measurement results and simulation of 2PASCL 4×4-bit array multiplier

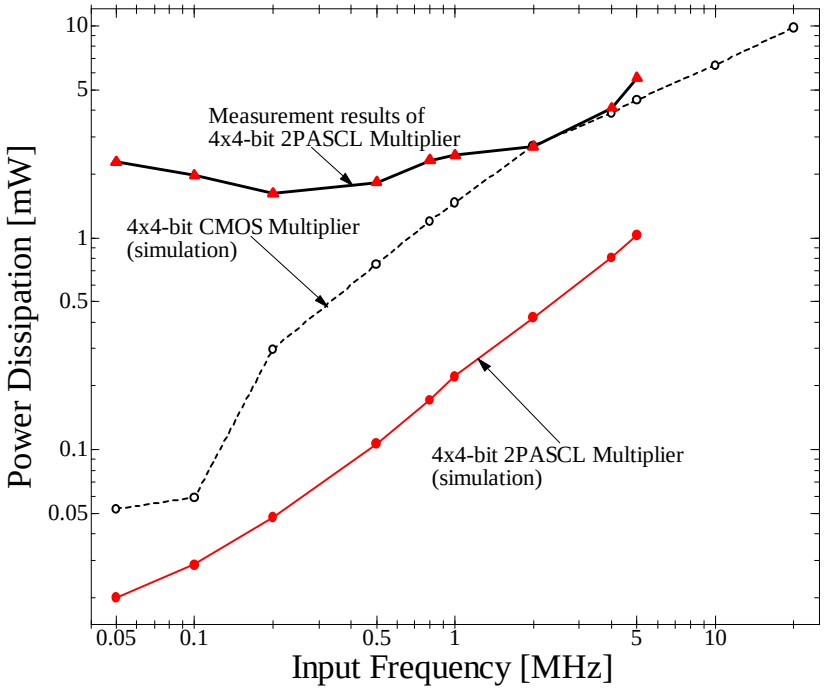

Fig. 1 Simulation results, comparison to CMOS multiplier and the actual measurement results after eliminating resistance power dissipation used to measure the current

2 On-resistance simulation and results

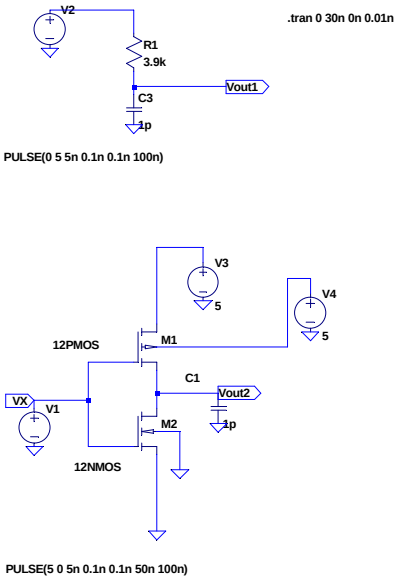

Fig. 2 LTSpice simulation diagram for calculation pMOS equivalent R_{on}

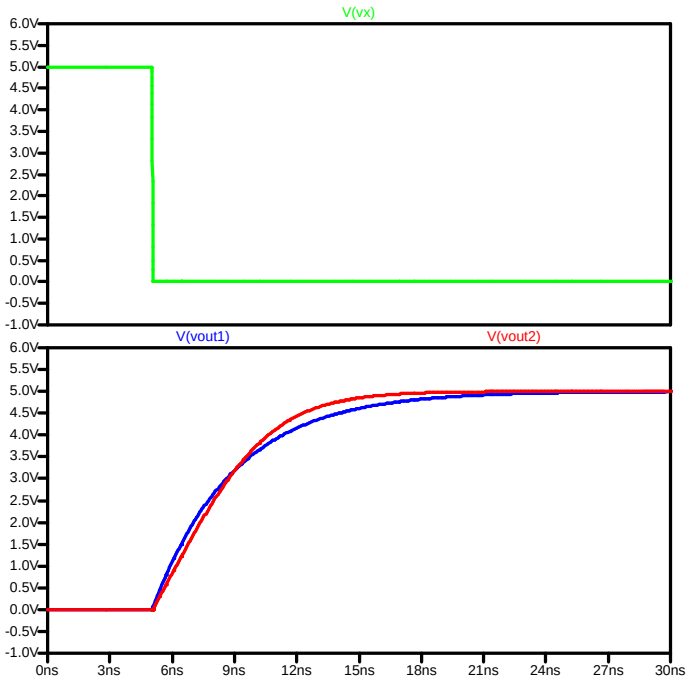

Fig. 3 pMOS R_{on} simulation results

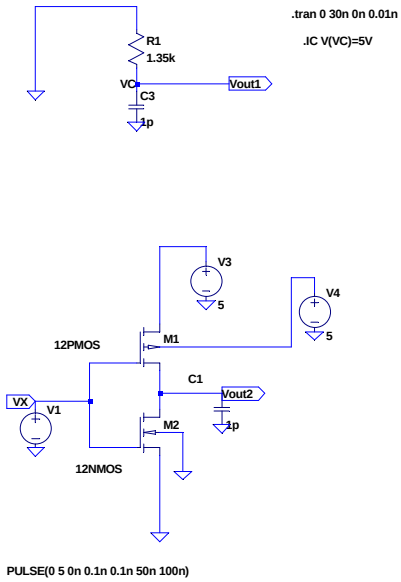

Fig. 4 LTSpice simulation diagram for calculation nMOS equivalent R_{on}

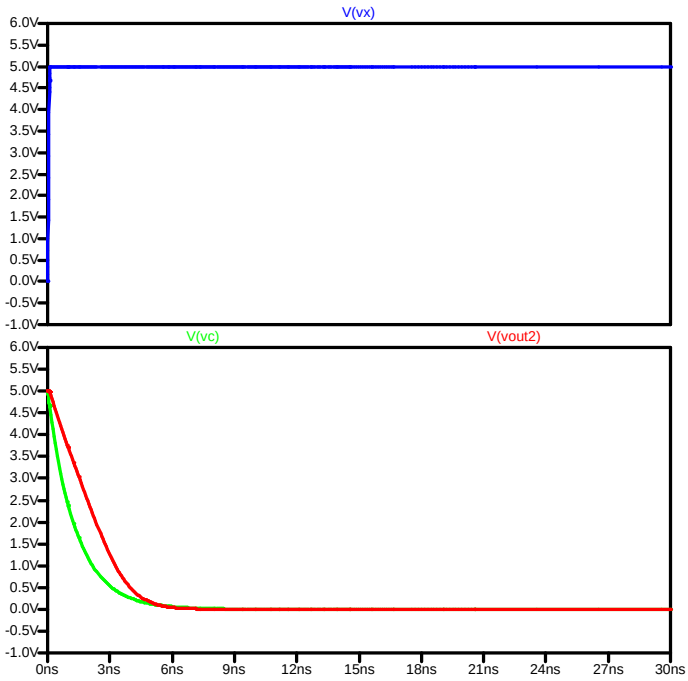

Fig. 5 nMOS R_{on} simulation results